ATTENTION

These devices contain circuits to protect the inputs and outputs against damage due to high static voltages or electrostatic fields; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits.

Unused inputs must always be connected to an appropriate logic voltage level, preferably either supply voltage or ground.

Additional information concerning the handling of ESD sensitive devices is provided in Section 12 in a document entitled *"Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies."*

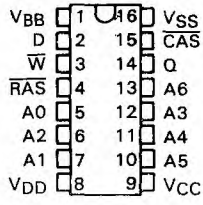
OCTOBER 1977—REVISED NOVEMBER 1985

- 16,384 X 1 Organization
- 10% Tolerance on All Supplies
- All Inputs Including Clocks TTL Compatible
- Unlatched Three-State Fully TTL-Compatible Output
- Performance Ranges:

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY-WRITE† CYCLE (MIN)
TMS4116-15	150 ns	100 ns	375 ns	375 ns
TMS4116-20	200 ns	135 ns	375 ns	375 ns
TMS4116-25	250 ns	165 ns	410 ns	515 ns

- Page-Mode Operation for Faster Access Time
- Common I/O Capability with Early Write Feature
- Low-Power Dissipation
  - Operating . . . 462 mW (Max)
  - Standby . . . 20 mW (Max)
- 1-T Cell Design, N-Channel Silicon-Gate Technology
- 16-Pin 300-Mil (7,62-mm) Package Configuration

N PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A6	Addresses
$\overline{CAS}$	Column-Address Strobe
D	Data Input
Q	Data Output
$\overline{RAS}$	Row-Address Strobe
V_{BB}	−5-V Power Supply
V_{CC}	5-V Power Supply
V_{DD}	12-V Power Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TMS4116 series is composed of monolithic high-speed dynamic 16,384-bit MOS random-access memories organized as 16,384 one-bit words, and employs single-transistor storage cells and N-channel silicon-gate technology.

All inputs and outputs are compatible with Series 74 TTL circuits including clocks: Row-Address Strobe $\overline{RAS}$ (or $\overline{R}$) and Column-Address Strobe $\overline{CAS}$ (or $\overline{C}$). All address lines (A0 through A6) and data in (D) are latched on chip to simplify system design. Data out (Q) is unlatched to allow greater system flexibility.

Typical power dissipation is less than 350 milliwatts active and 6 milliwatts during standby (V_{CC} is not required during standby operation). To retain data, only 10 milliwatts average power is required which includes the power consumed to refresh the contents of the memory.

The TMS4116 series is offered in a 16-pin dual-in-line plastic (N suffix) package and is guaranteed for operation from 0°C to 70°C. The package is designed for insertion in mounting-hole rows on 7,62-mm (300-mil) centers.

operation

address (A0-A6)

Fourteen address bits are required to decode 1 of 16,384 storage cell locations. Seven row-address bits are set up on pins A0 through A6 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the

†The term "read-write cycle" is sometimes used as an alternative to "read-modify-write cycle."

seven column-address bits are set up on pins A0 through A6 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in ($\overline{D}$)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle, the output goes active after the enable time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In an early write cycle, the output is always in the high-impedance state. In a delayed-write or read-modify-write cycle, the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least every two milliseconds to retain data. Since the output buffer is in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 128 row addresses (A0 through A6) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ remains high (inactive) for this refresh sequence, thus conserving power.

page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses on the same page is eliminated. To extend beyond the 128 column locations on a single RAM, the row address and $\overline{RAS}$ is applied to multiple 16K RAMs; $\overline{CAS}$ is decoded to select the proper RAM.

power up

V_{BB} must be applied to the device either before or at the same time as the other supplies and removed last. Failure to observe this precaution will cause dissipation in excess of the absolute maximum ratings due to internal forward bias conditions. This also applies to system use, where failure of the V_{BB} supply must immediately shut down the other supplies. After power up, eight $\overline{RAS}$ cycles must be performed to achieve proper device operation.

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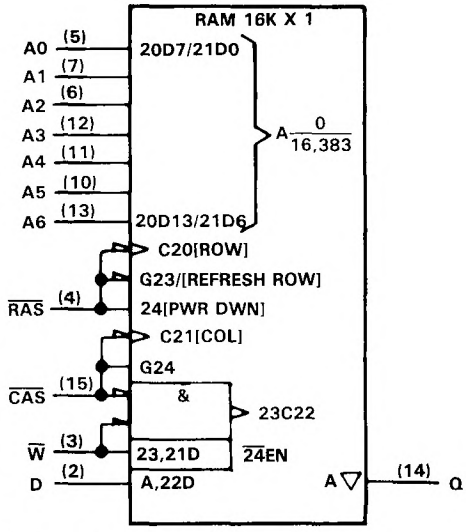
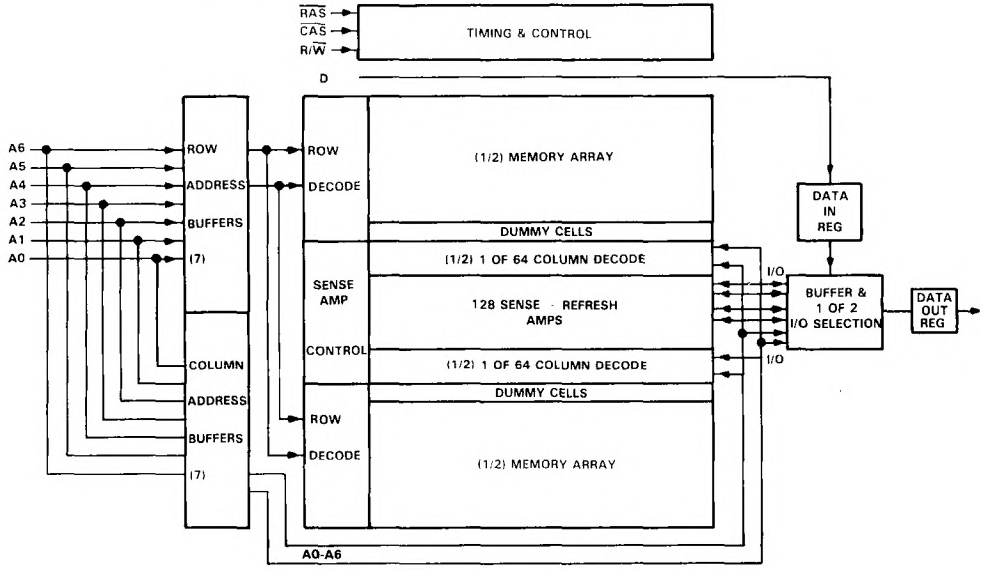
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage on any pin (see Note 1) . . . . . −0.5 V to 20 V
Voltage on V_{CC}, V_{DD} supplies with respect to V_{SS} . . . . . −1 V to 15 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this data sheet, voltage values are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{BB}	Supply voltage		−4.5	−5	−5.5	V
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{DD}	Supply voltage		10.8	12	13.2	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	All inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$	2.4		7	V
		$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$	2.7		7	
V_{IL}	Low-level input voltage (see Note 2)		−1	0	0.8	V
T_A	Operating free-air temperature		0		70	°C

NOTE 2: The algebraic convention, whera the more negative (less positive) limit is designated as maximum, is used in this data sheet for logic voltage only.

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electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 7 V, All other pins = 0 V except V_{BB} = −5 V			10	μA
I_O	Output current (leakage)	V_O = 0 to 5.5 V, $\overline{CAS}$ high			±10	μA
I_{BB1}	Average operating current during read or write cycle	Minimum cycle time		50	200	μA
I_{CC1}‡					4§	mA
I_{DD1}				27	35	mA
I_{BB2}	Standby current	After 1 memory cycle $\overline{RAS}$ and $\overline{CAS}$ high		10	100	μA
I_{CC2}					±10	μA
I_{DD2}				0.5	1.5	mA
I_{BB3}	Average refresh current	Minimum cycle time $\overline{RAS}$ cycling, $\overline{CAS}$ high		50	200	μA
I_{CC3}					±10	μA
I_{DD3}				20	27	mA
I_{BB4}	Average page-mode current	Minimum cycle time $\overline{RAS}$ low, $\overline{CAS}$ cycling		50	200	μA
I_{CC4}‡					4§	mA
I_{DD4}				20	27	mA

† All typical values are at T_A = 25°C and nominal supply voltages.
‡ V_{CC} is applied only to the output buffer, so I_{CC} depends on output loading.
§ Output loading two standard TTL loads.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		TYP†	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs	4	5	pF
$C_{i(D)}$	Input capacitance, data input	4	5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs	8	10	pF
$C_{i(W)}$	Input capacitance, write enable input	8	10	pF
C_o	Output capacitance	5	7	pF

switching characteristics over recommended supply voltage range and operating free-air temperature range

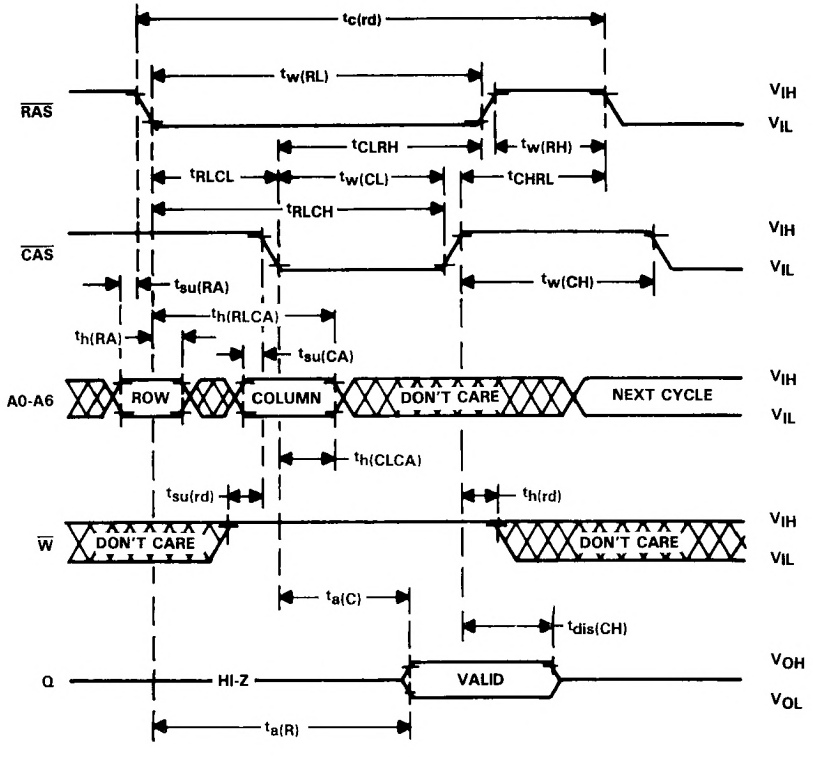
PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS4116-15		TMS4116-20		TMS4116-25		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		100		135		165	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF, Load = 2 Series, 74 TTL gates	t_{RAC}		150		200		250	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	40	0	50	0	60	ns

† All typical values are at T_A = 25°C and nominal supply voltages.

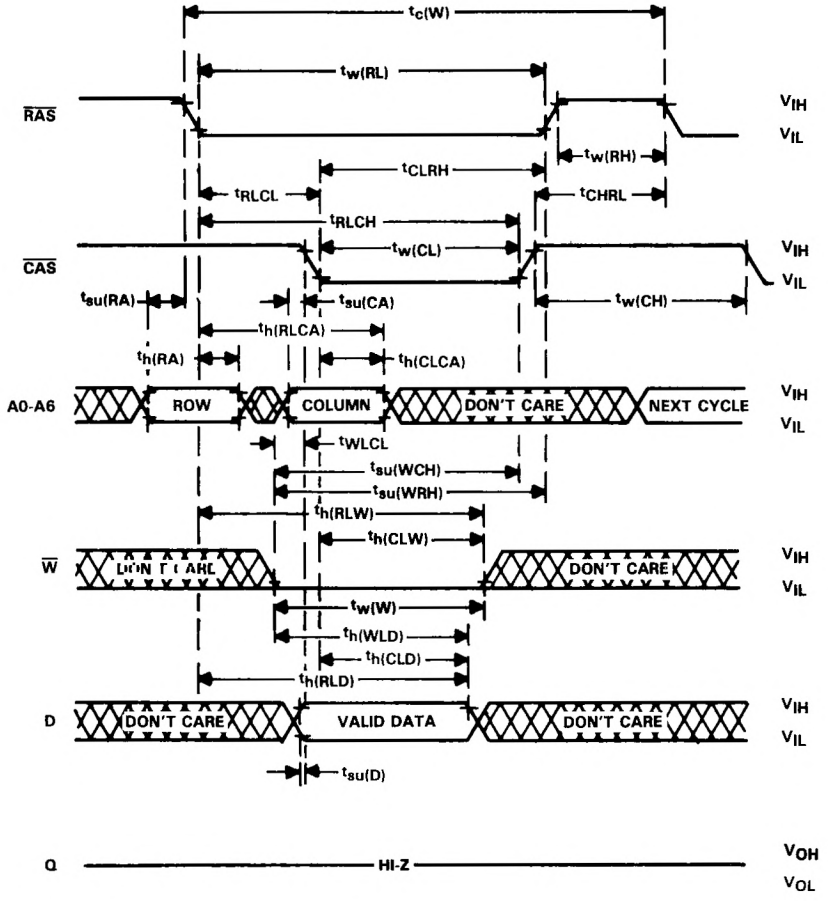
timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TMS4116-15 MIN	TMS4116-15 MAX	TMS4116-20 MIN	TMS4116-20 MAX	TMS4116-25 MIN	TMS4116-25 MAX	UNIT
$t_{c(P)}$	Page-mode cycle time	t_{PC}	170						ns
$t_{c(rd)}$	Read cycle time	t_{RC}	375		375		410		ns
$t_{c(W)}$	Write cycle time	t_{WC}	375		375		410		ns
$t_{c(rdW)}$	Read-modify-write cycle time	t_{RWC}	375		375		515		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time)	t_{CP}	60		80		100		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low	t_{CAS}	100	10,000	135	10,000	165	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	100		120		150		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low	t_{RAS}	150	10,000	200	10,000	250	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	45		55		75		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and CAS	t_T	3	35	3	50	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	−10		−10		−10		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	60		80		100		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	60		80		100		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	45		55		75		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	20		25		35		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	95		120		160		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DHC}	45		55		75		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	95		120		160		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DHW}	45		55		75		ns
$t_{h(rd)}$	Read-command hold time	t_{RCH}	0		0		0		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	45		55		75		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	95		120		160		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		200		250		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	−20		−20		−20		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	100		135		165		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write-cycle only)	t_{CWD}	70		95		125		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	20	50	25	65	35	85	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write-cycle only)	t_{RWD}	120		160		200		ns
t_{WLCL}	Delay time, W low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	−20		−20		−20		ns
t_{rf}	Refresh time interval	t_{REF}		2		2		2	ms

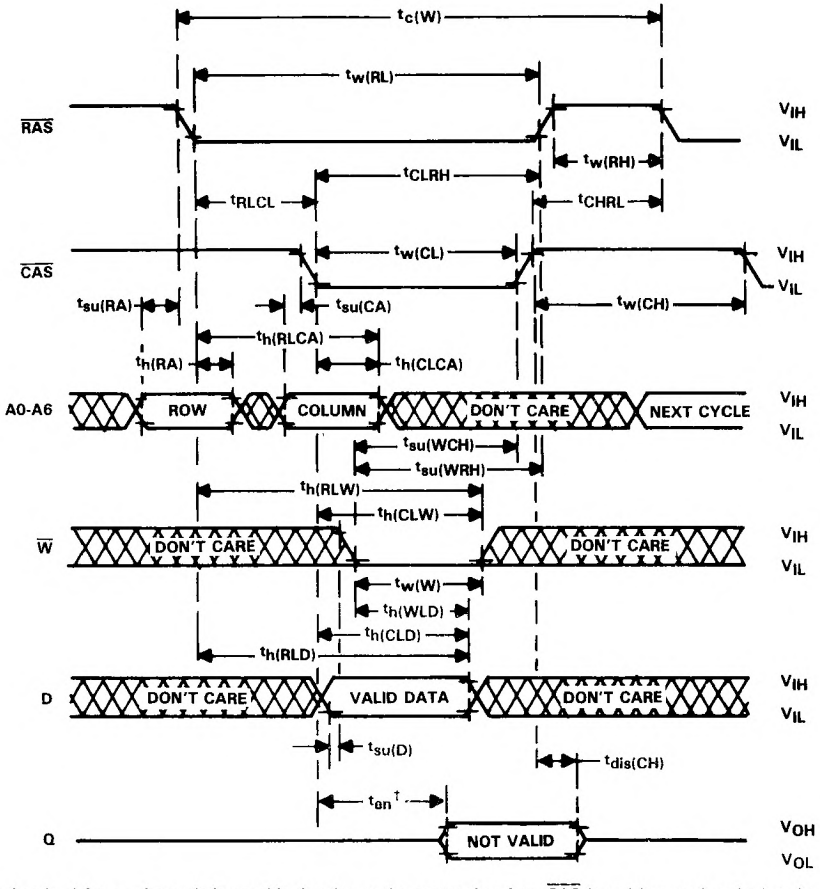
read cycle timing



early write cycle timing

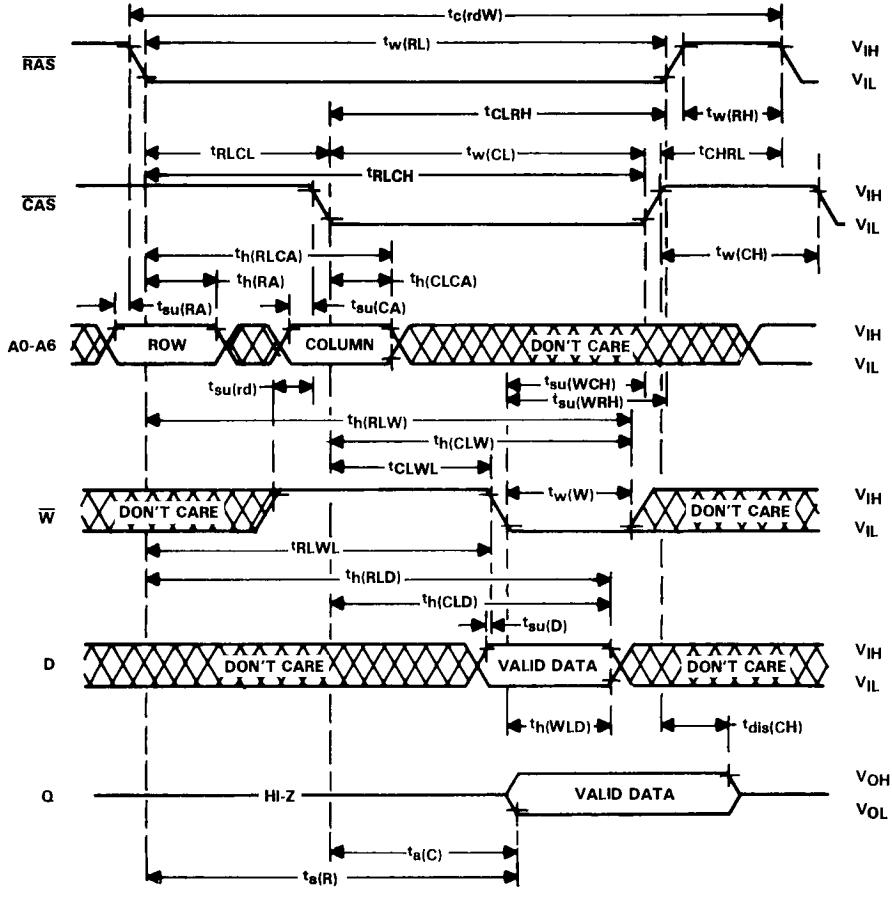


write cycle timing



† The enable time (t_{en}) for a write cycle is equal in duration to the access time from $\overline{CAS}$ ($t_{a(C)}$) in a read cycle; but the same active levels at the output are invalid.

read-write/read-modify-write cycle timing



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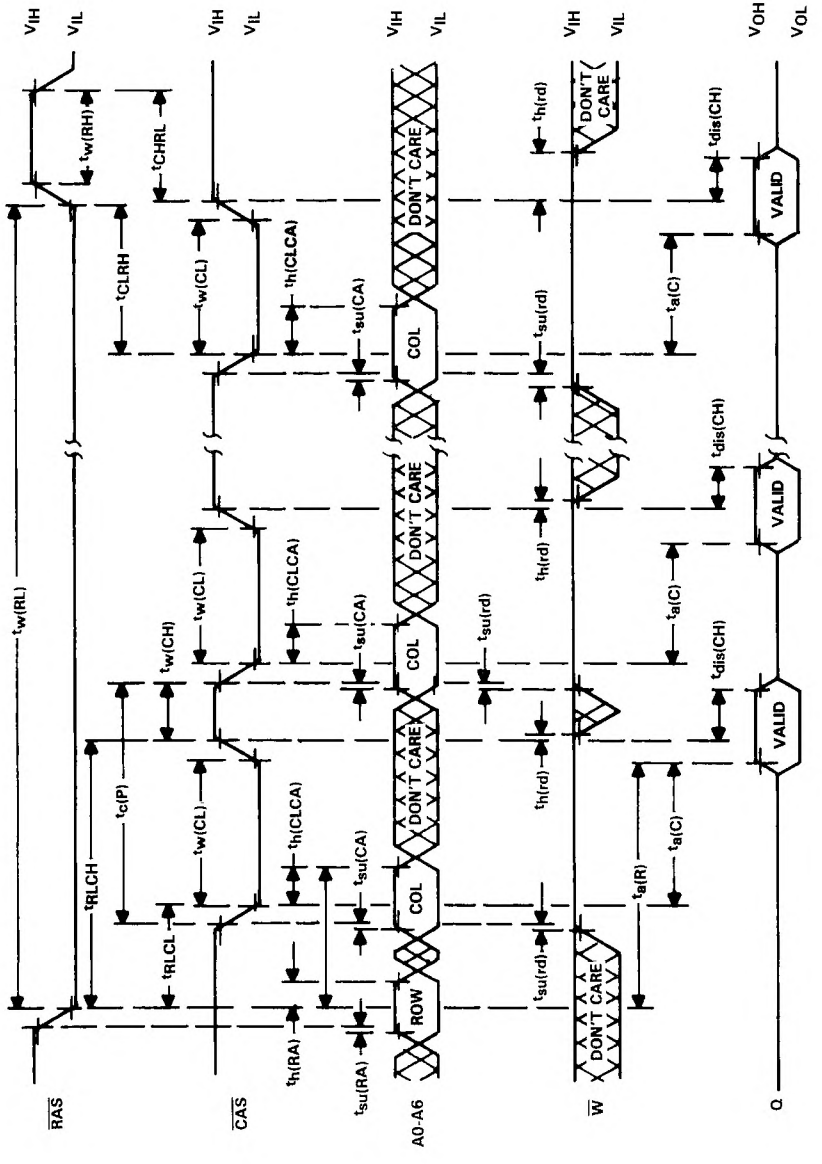
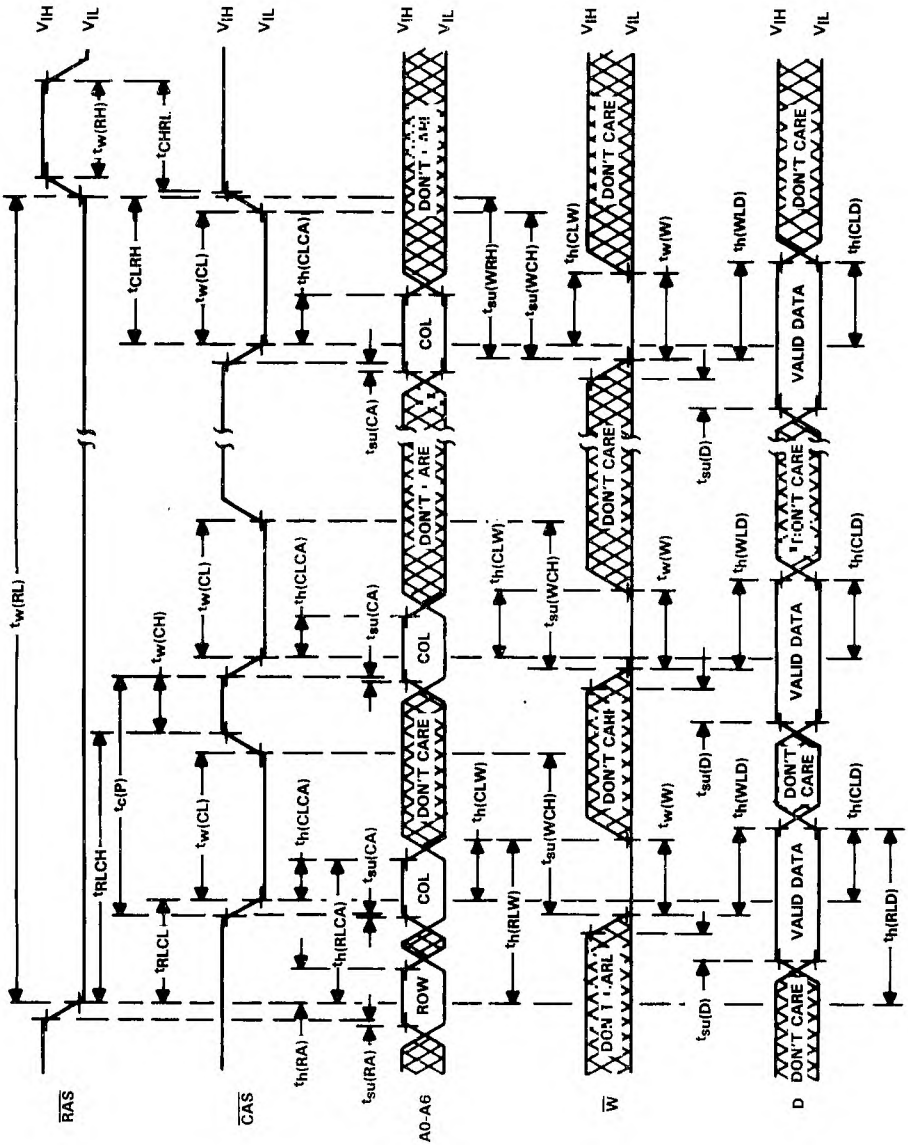
page-mode read cycle timing



page-mode write cycle timing



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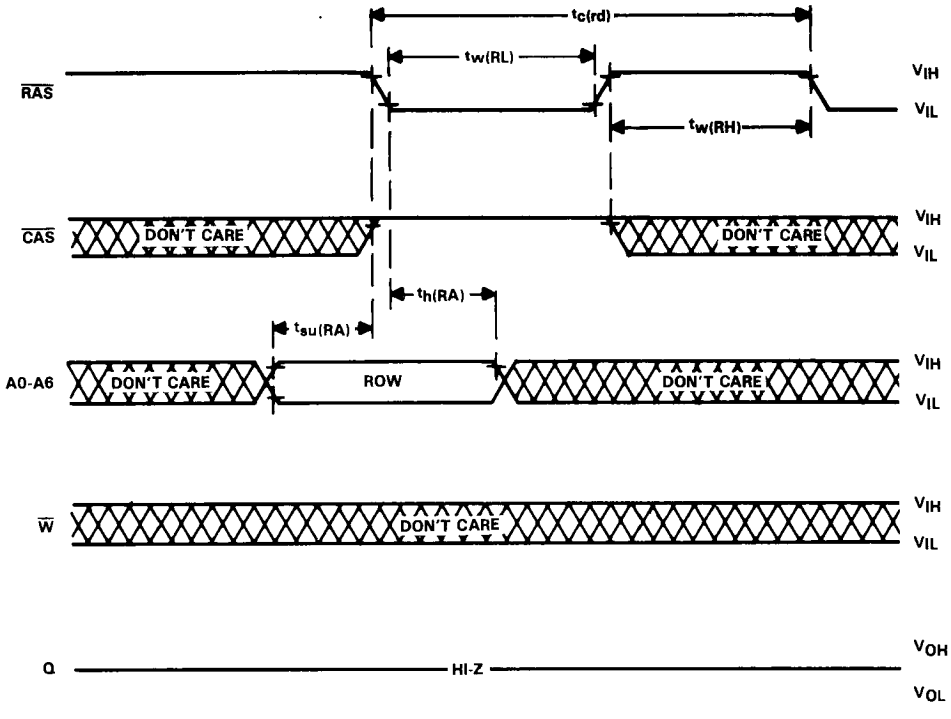
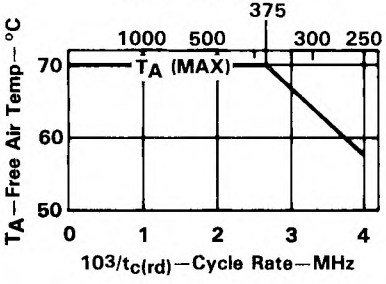
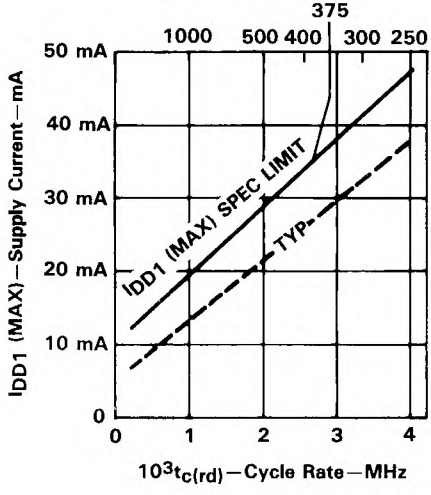
$\overline{\text{RAS}}$-only refresh timing



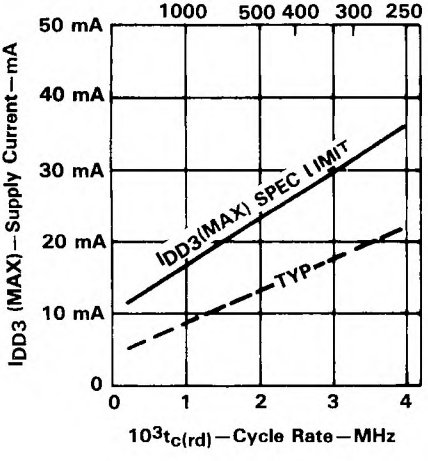
CYCLE RATE (& TIME)
vs
TEMPERATURE



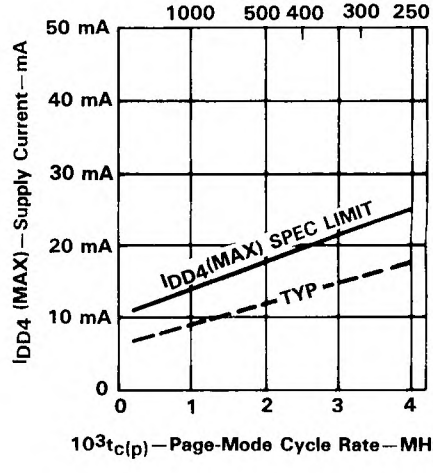
CYCLE RATE (& TIME)
vs
MAX SUPPLY CURRENT, I_{DD1}



CYCLE RATE (& TIME)
vs
MAX SUPPLY CURRENT, I_{DD3}



PAGE-MODE CYCLE RATE (& TIME)
vs
MAX SUPPLY CURRENT, I_{DD4}



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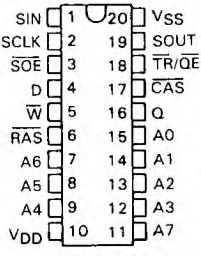
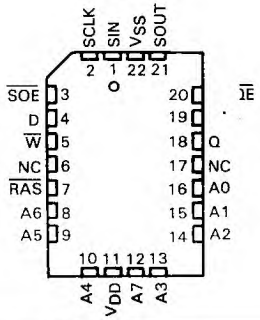
JULY . ED NOVEMBER 1985

- Dual Accessibility — One Port Sequential Access, One Port Random Access
- Four Cascaded 64-Bit Serial Shift Registers for Sequential Access Applications
- Designed for Both Video and Non-Video Applications
- Fast Serial Port . . . Can Be Configured for Video Data Rates in Excess of 150 MHz
- $\overline{TR}/\overline{QE}$ as Output Enable Allows Direct Connection of D, Q and Address Lines to Simplify System Design
- Random Access Port Looks Exactly Like a TMS4164
- Separate Serial In and Serial Out to Allow Simultaneous Shift In and Out
- 65,536 × 1 Organization
- Supported by TI's TMS34061 Video System Controller (VSC)
- Maximum Access Time from $\overline{RAS}$ Less Than 150 ns
- Minimum Cycle Time (Read or Write) Less Than 240 ns
- Long Refresh Period . . . 4 ms
- Low Refresh Overhead Time . . . As Low As 1.7% of Total Refresh Period
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Unlatched Outputs for Both Random and Serial Access
- Common I/O Capability with "Early Write" Feature
- Page-Mode Operation for Faster Access
- Low Power Dissipation (TMS4161-15)
  —Operating . . . 250 mW (Typical)
  —Standby . . . 80 mW (Typical)
- New SMOS (Scaled-MOS) N-Channel Technology
- $\overline{SOE}$ Simplifies Multiplexing of Serial Data Streams
- Available with MIL-STD-883B Processing and L(0°C to 70°C), E(−40°C to 85°C), or S(−55°C to 100°C) Temperature Ranges

N PACKAGE
(TOP VIEW)



FM PACKAGE
(TOP VIEW)



PIN NOMENCLATURE			
A0-A7	Address Inputs	SIN	Serial Data In
$\overline{CAS}$	Column-Address Strobe	$\overline{SOE}$	Serial Output Enable
D	Random-Access Data In	SOUT	Serial Data Out
		$\overline{TR}/\overline{QE}$	Register Transfer/ Q Output Enable
NC	No Connection		
Q	Random-Access Data Out	V_{DD}	5-V Supply
		V_{SS}	Ground
$\overline{RAS}$	Row-Address Strobe	$\overline{W}$	Write Enable
SCLK	Serial Data Clock		

description

The TMS4161 is a high-speed, dual-access 65,536-bit dynamic random-access memory. The random-access port makes the memory look like it is organized as 65,536 words of one bit each like the TMS4164. The sequential access port is interfaced to an internal 256-bit dynamic shift register organized as four cascaded 64-bit shift registers which makes the memory look like it is organized as up to 256 words of up to 256 bits each which are accessed serially. One, two, three, or four 64-bit shift registers can be sequentially read out after a transfer cycle depending on a two-bit code applied to the two most significant column address inputs. The TMS4161 employs state-of-the-art SMOS (Scaled-MOS) N-channel double-level polysilicon gate technology for very high performance combined with low cost and improved reliability.

The TMS4161 features full asynchronous dual access capability except when transferring data between the shift register and the memory array.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power. Note that the transfer of a row of data from the memory array to the shift register also refreshes that row.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS4161 is offered in 20-pin plastic dual-in-line and 22-pin plastic chip carrier packages. It is guaranteed for operation from 0°C to 70°C. The dual-in-line package is designed for insertion in mounting-hole rows on 7,62-mm (300-mil) centers.

random access address space to sequential address space mapping

The TMS4161 is designed with each row divided into four, 64-column sections (see functional block diagram). The first column section to be shifted out is selected by the two most significant column address bits. If the two bits represent binary 00, then one to four registers can be shifted out in order. If the two bits represent binary 01, then only 1 to 3 (the most significant) registers can be shifted out in order. If the two bits represent 10, then one to two of the most significant registers can be shifted out in order. Finally, if the two bits represent 11 only the most significant register can be shifted out. All registers are shifted out with the least significant bit (bit 0) first and the most significant bit (bit 63) last. Note that if the two column address bits equal 00 during the last register transfer cycle ($\overline{TR}/\overline{QE}$ at logic level "0" as $\overline{RAS}$ falls) a total of 256 bits can be sequentially read out.

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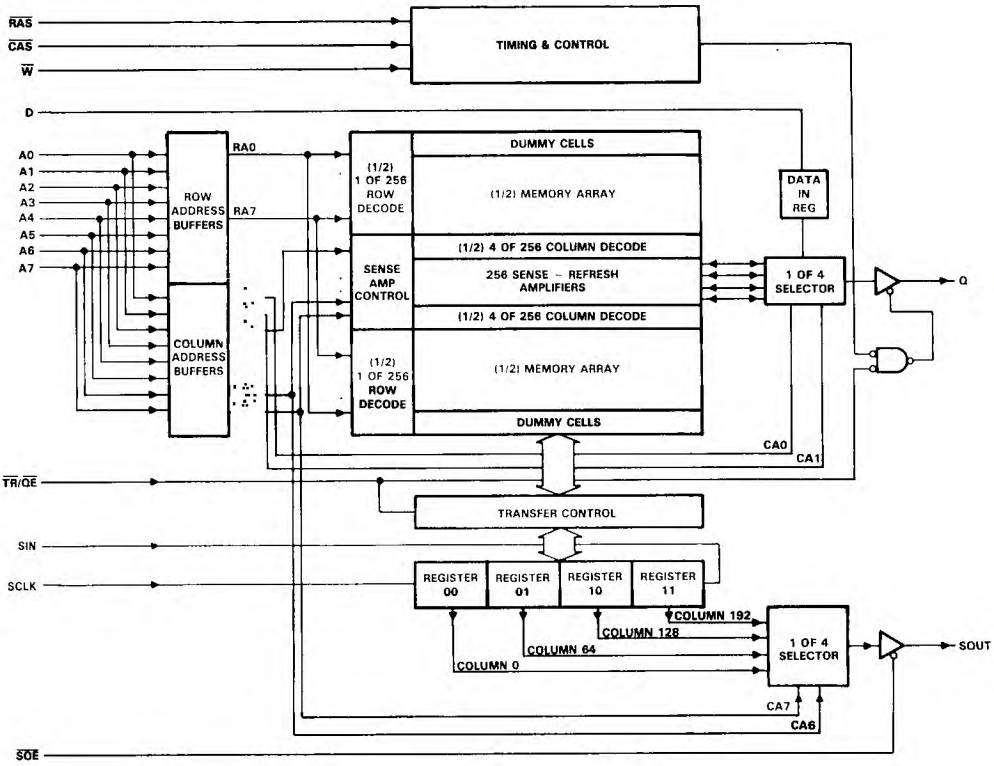
functional block diagram



random-access operation

TR/QE

The TR/QE pin has two functions. First, it selects either register transfer or random-access operation as RAS falls, and second, if this is a random-access operation, it functions as an output enable after CAS falls.

To use the TMS4161 in the random-access mode, TR/QE must be high as RAS falls. Holding TR/QE high as RAS falls keeps the 256 elements of the shift registers disconnected from the corresponding 256 bit lines of the memory array. If data is to be shifted, the shift registers must be disconnected from the bit lines. Holding TR/QE low as RAS falls enables the 256 switches that connect the shift registers to the bit lines and indicates that a transfer will occur between the shift registers and one of the memory rows.

During random-access operation, once CAS has been pulled low, TR/QE controls when the data will appear at the Q output (if this is a read cycle). Whenever TR/QE is held high during random-access operation, the Q output will be in the high-impedance state. This feature removes the possibility of an overlap between data on the address lines and data appearing on the Q output making it possible to connect the address lines to the Q and D lines (Use of this organization prohibits the use of the early write cycle.).

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage cell locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable (W) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data out will remain inthe high-impedance state for the entire cycle permitting common I/O operation.

data in (D)

Data is written during a write or read-modify-write cycle. The falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state as long as $\overline{CAS}$ or $\overline{TR}$ is held high. Data will not appear on the output until after both $\overline{CAS}$ and $\overline{TR}/\overline{QE}$ have been brought low. In a read cycle, the guaranteed maximum output enable access time is valid only if t_{CQE} is greater than t_{CQE} MAX, and t_{RLCL} is greater than t_{RLCL} MAX. Likewise, $t_{a(C)}$ MAX is valid only if t_{RLCL} is greater than t_{RLCL} MAX. Once the output is valid, it will remain valid while $\overline{CAS}$ and $\overline{TR}/\overline{QE}$ are both low; $\overline{CAS}$ or $\overline{TR}$ going high will return the output to a high-impedance state. In an early write cycle, the output is always in a high-impedance state. In a delayed write or ready-modify-write cycle, the output will follow the sequence for the read cycle. In a register transfer cycle, the output will always be in a high-impedance state.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffer is in high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on a single RAM, the row address and $\overline{RAS}$ are applied to multiple 64K RAMs. $\overline{CAS}$ is then decoded to select the proper RAM.

power up

After power up, the power supply must remain at its steady-state value for 1 ms. In addition, $\overline{RAS}$ must remain high for 100 μs immediately prior to initialization. Initialization consists of performing eight $\overline{RAS}$ cycles before proper device operation is achieved.

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sequential-access operation

$\overline{TR}/\overline{QE}$

Memory transfer operations involving parallel use of the shift register are first indicated by bringing $\overline{TR}/\overline{QE}$ low before $\overline{RAS}$ falls low. This enables the switches connecting the 256 elements of the shift register to the 256 bit lines of the memory array. The $\overline{W}$ line determines whether the data will be transferred from or to the shift registers.

write enable ($\overline{W}$)

In the sequential access mode, $\overline{W}$ determines whether a transfer will occur from the shift registers to the memory array, or from the memory array to the shift registers. To transfer from the shift registers to the memory array, $\overline{W}$ is held low as $\overline{RAS}$ falls, and, to transfer from the memory array to the shift registers, $\overline{W}$ is held high as $\overline{RAS}$ falls. Thus, reads and writes are always with respect to the memory array. The write setup and hold times are referenced to the falling edge of $\overline{RAS}$ for this mode of operation.

row address (A0 through A7)

Eight address bits are required to select one of the 256 possible rows involved in the transfer of data to or from the shift registers. A0-A7, $\overline{W}$, and $\overline{TR}/\overline{QE}$ are latched on the falling edge of $\overline{RAS}$.

register column address (A7, A6)

To select one of the four shift registers (transfer from memory to register only), the appropriate 2-bit column address (A7, A6) must be valid when $\overline{CAS}$ falls. However, the $\overline{CAS}$ and register address signals need not be supplied every transfer cycle, only when it is desired to change or select a new register.

SCLK

Data is shifted in and out on the rising edge of SCLK. This makes it possible to view the shift registers as though it were made of 256 rising edge D flip-flops connected D to Q. The TMS4161 is designed to work with a wide range duty cycle clock to simplify system design. Note that data will appear at the SOUT pin not only on the rising edge of SCLK but also after an access time of $t_{a(RSO)}$ from $\overline{RAS}$ high during a parallel load of the shift registers.

SIN and SOUT

Data is shifted in through the SIN pin and is shifted out through the SOUT pin. The TMS4161 is designed such that it requires 3 ns hold time on SIN as SCLK rises. SOUT is guaranteed not to change for at least 8 ns after SLCK rises. These features make it possible to easily connect TMS4161s together, to allow SOUT to be connected to SIN, and to give external circuitry a full SLCK cycle time to allow manipulation of the serial data. When loading data into the shift register from the serial input in preparation for a shift register to memory transfer operation, the serial clock must be clocked an even number of times. To guarantee proper serial clock sequence after power up, a transfer cycle must be initiated before a serial data stream is applied at SIN.

$\overline{SOE}$

The serial output enable pin controls the impedance of the serial output, allowing multiplexing of more than one bank of TMS4161 memories into the same external video circuitry. When $\overline{SOE}$ is at a logic low level, SOUT will be enabled and the proper data read out. When $\overline{SOE}$ is at a logic high level, SOUT will be disabled and be in the high-impedance state.

refresh

The shift registers are also dynamic storage elements. The data held in the registers will be lost unless SCLK goes high to shift the data one bit position, a transfer write operation is invoked, or the data is reloaded from the memory array. See specifications for maximum register data retention times. Important: If the shift register has remained idle for a time period which exceeds the maximum SCLK high or SCLK low time, the dynamic clock circuits will also lose charge. Under these conditions, the shift register clocks must be re-enabled by performing any transfer cycle before data can be shifted into or out of the shift register.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin except V_{DD} and data out (see Note 1) . . . . . −1.5 V to 10 V
Voltage range on V_{DD} supply and data out with respect to V_{SS} . . . . . −1 V to 6 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		$V_{DD}+0.3$	V
V_{IL}	Low-level input voltage (see Notes 2 and 3)	−0.6		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTES: 2. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.
3. Due to input protection circuitry, the applied voltage may begin to clamp at −0.6 V; test conditions must comprehend this occurrence.
4. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.

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electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS4161-15			TMS4161-20			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage (Q, SOUT)	I_{OH} = −5 mA	2.4			2.4			V
V_{OL}	Low-level output voltage (Q, SOUT)	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All other pins = 0 V			±10			±10	μA
I_O	Output current (leakage) (Q, SOUT)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V			±10			±10	μA
I_{DD1}	Average operating current during read or write cycle	$t_{c(P)}$ = minimum cycle time, $\overline{TR}/\overline{QE}$ low after $\overline{RAS}$ falls,‡ SCLK and SIN low, $\overline{SOE}$ high, No load on Q and SOUT		50	70		50	70	mA
I_{DD2}§	Standby current	After 1 $\overline{RAS}$ cycle, $\overline{RAS}$ and $\overline{CAS}$ high, SCLK and SIN low, $\overline{SOE}$ high, No load on Q and SOUT		16	20		16	20	mA
I_{DD3}	Average refresh current	$t_{c(rf)}$ = minimum cycle time, $\overline{TR}/\overline{QE}$ high, $\overline{RAS}$ cycling, SCLK and SIN low, $\overline{SOE}$ high, $\overline{TR}/\overline{QE}$ high, No load on Q and SOUT		42	55		37	50	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle time, $\overline{RAS}$ low, $\overline{CAS}$ cycling, $\overline{TR}/\overline{QE}$ low after $\overline{RAS}$ falls, SCLK and SIN low, $\overline{SOE}$ high, No load on Q and SOUT		45	55		40	50	mA
I_{DD5}	Average shift register current (includes I_{DD2})	$\overline{RAS}$ and $\overline{CAS}$ high, No load on Q and SOUT, $t_{c(SCLK)} = t_{c(SCLK)}$ min		30	40		30	40	mA
I_{DD6}	Worst case average DRAM and shift register current	$t_{c(rd)}$ = minimum cycle time, $t_{c(SCLK)}$ = minimum cycle time, $\overline{TR}/\overline{QE}$ low after $\overline{RAS}$ falls, No load on Q and SOUT		85	95		80	90	mA

NOTE 5: Additional information on I_{DD1} – I_{DD6} on page 4-40.
† All typical values are at T_A = 25°C and nominal supply voltages.
‡ See appropriate timing diagram.
§ V_{IL} > −0.6 V.

capacitance over recommended supply voltage and operating free-air temperature range, f = 1 MHz

PARAMETER		TYP†	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs	4	5	pF
$C_{i(D)}$	Input capacitance, data input	4	5	
$C_{i(RC)}$	Input capacitance, strobe inputs	8	10	
$C_{i(W)}$	Input capacitance, write enable input	8	10	
$C_{i(CK)}$	Input capacitance, serial clock	8	10	
$C_{i(SI)}$	Input capacitance, serial in	4	5	
$C_{i(SOE)}$	Input capacitance, serial output enable	4	5	
$C_{i(TR)}$	Input capacitance, register transfer input	4	5	
$C_{o(Q)}$	Output capacitance, random-access data	5	7	
$C_{o(SOUT)}$	Output capacitance, serial out	5	7	

† All typical values are at T_A = 25°C and nominal supply voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range (see Figure 1)

PARAMETER		TEST CONDITIONS†	ALT. SYMBOL	TMS4161-15		TMS4161-20		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF	t_{CAC}		100		135	ns
$t_{a(QE)}$	Access time of Q from $\overline{TR}/\overline{QE}$ low	C_L = 100 pF			40		50	
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF	t_{RAC}		150		200	
$t_{a(RSO)}$	SOUT access time from $\overline{SC}$ high	C_L = 30 pF			65		85	
$t_{a(SOE)}$	Access time from $\overline{SOE}$ low to SOUT	C_L = 30 pF			20		25	
$t_{a(SO)}$	Access time from SCLK	C_L = 30 pF			45		50	
$t_{dis(CH)}$‡	Q output disable time from $\overline{CAS}$ high	C_L = 100 pF	t_{OFF}		40		40	
$t_{dis(QE)}$‡	Q output disable time from $\overline{TR}/\overline{QE}$ high	C_L = 100 pF			30		40	
$t_{dis(SOE)}$‡	Serial output disable time from $\overline{SOE}$ high	C_L = 30 pF			20		25	

† Figure 1 shows the load circuit.
‡ The maximum values for $t_{dis(CH)}$, $t_{dis(QE)}$, and $t_{dis(SOE)}$ define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL}.

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timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TMS4161-15		TMS4161-20		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time	t_{PC}	160		225		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	240		315		ns
$t_{c(W)}$	Write cycle time	t_{WC}	240		315		ns
$t_{c(TW)}$	Transfer write cycle time‡		240		315		ns
$t_{c(Trd)}$	Transfer read cycle time		240		315		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	265		330		ns
$t_{c(SCLK)}$	Serial-clock cycle time	t_{SCC}	45	50,000	50	50,000	ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time§	t_{CP}	50		80		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low¶	t_{CAS}	100	10,000	135	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	80		105		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low#	t_{RAS}	150	10,000	200	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	45		45		ns
$t_{w(CKL)}$	Pulse duration, SCLK low		10		10		ns
$t_{w(CKH)}$	Pulse duration, SCLK high		12		12		ns
$t_{w(QE)}$	$\overline{TR}/\overline{QE}$ pulse duration low time (read cycle)		40		40		ns
t_t	Transition times (rise and fall) $\overline{RAS}$, $\overline{CAS}$, and SCLK	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(RW)}$	$\overline{W}$ setup time before $\overline{RAS}$ low with $\overline{TR}/\overline{QE}$ low		0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCL)}$	Early write-command setup time before $\overline{CAS}$ low	t_{WCS}	−5		−5		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	40		60		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	40		60		ns
$t_{su(TR)}$	$\overline{TR}/\overline{QE}$ setup time before $\overline{RAS}$ low		0		0		ns
$t_{su(SI)}$	Serial-data setup time before SCLK high		6		6		ns
$t_{h(SI)}$	Serial-data-in hold time after SCLK high		3		3		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	45		55		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	20		25		ns
$t_{h(RW)}$	$\overline{W}$ hold time after $\overline{RAS}$ low with $\overline{TR}/\overline{QE}$ low		20		20		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	95		120		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	60		80		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	110		145		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	45		55		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns

(Continued next page.)

NOTE 6: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

†All cycle times assume t_t = 5 ns except $t_{c(SCLK)}$ which assumes t_t = 3 ns.

‡Multiple transfer write cycles require separation by either a 500 ns $\overline{RAS}$-precharge interval or any other active $\overline{RAS}$-cycle.

§Page-mode only.

¶In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{W(CL)}$). This applies to page-mode read-modify-write also.

#In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{W(RL)}$).

timing requirements over recommended supply voltage range and operating free-air temperature range (concluded)

		ALT. SYMBOL	TMS4161-15		TMS4161-20		UNIT
			MIN	MAX	MIN	MAX	
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	5		5		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	60		80		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	110		145		ns
$t_{h(RSO)}$	Serial-data-out hold time after $\overline{RAS}$ low with $\overline{TR}/\overline{QE}$ low		30		30		ns
$t_{h(SO)}$	Serial-data-out hold time after SCLK high		8		8		ns
$t_{h(TR)}$	$\overline{TR}/\overline{QE}$ hold time after $\overline{RAS}$ low (transfer)		20		20		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLQEH}	Delay time, $\overline{CAS}$ low to $\overline{QE}$ high		100		135		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	100		135		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	65		75		ns
t_{CQE}	Delay time, [illegible] ow to $\overline{QE}$ low (maximum value specified only to guarantee $t_{a(QE)}$ access time)			60		85	ns
t_{RHSC}	Delay time, $\overline{RAS}$ high to SCLK high		80	50,000	80	50,000	ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	50	30	65	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	135		150		ns
t_{CKRL}	Delay time, SCLK high before $\overline{RAS}$ low with $\overline{TR}/\overline{QE}$ low‖		10	50,000	10	50,000	ns
$t_{rf(MA)}$	Refresh time interval, memory array	t_{REF1}		4		4	ms
$t_{rf(SR)}$	Refresh time interval, shift register☆	t_{REF2}		50,000		50,000	ns

NOTE 6: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

‖SCLK may be high or low during $t_{w(RL)}$, but there can not be any positive edge transitions on SCLK for a minimum of 10 ns prior to $\overline{RAS}$ going low with $\overline{TR}/\overline{QE}$ low (i.e., before a transfer cycle).

☆See "refresh" on page 4-22.

PARAMETER MEASUREMENT INFORMATION

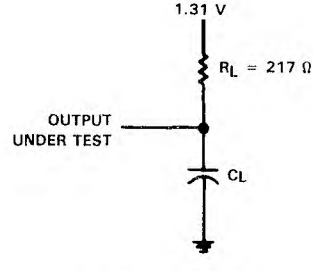

FIGURE 1. LOAD CIRCUIT

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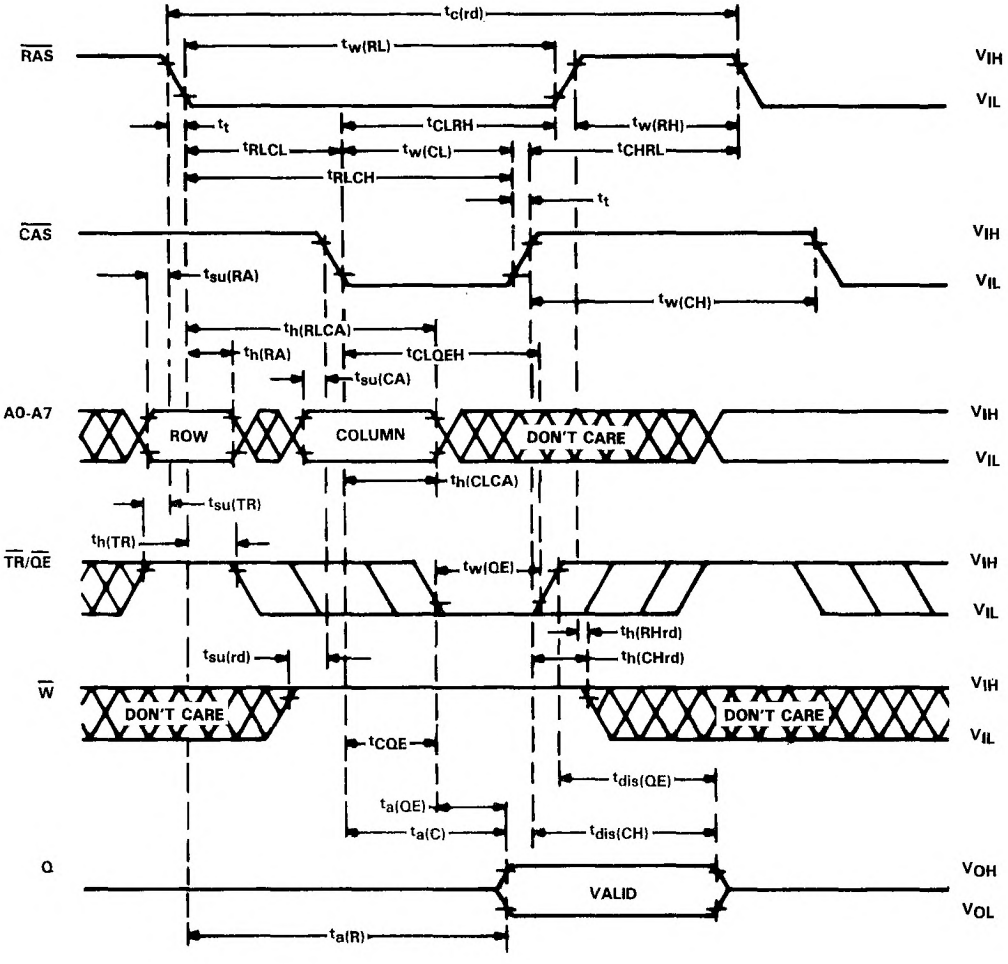
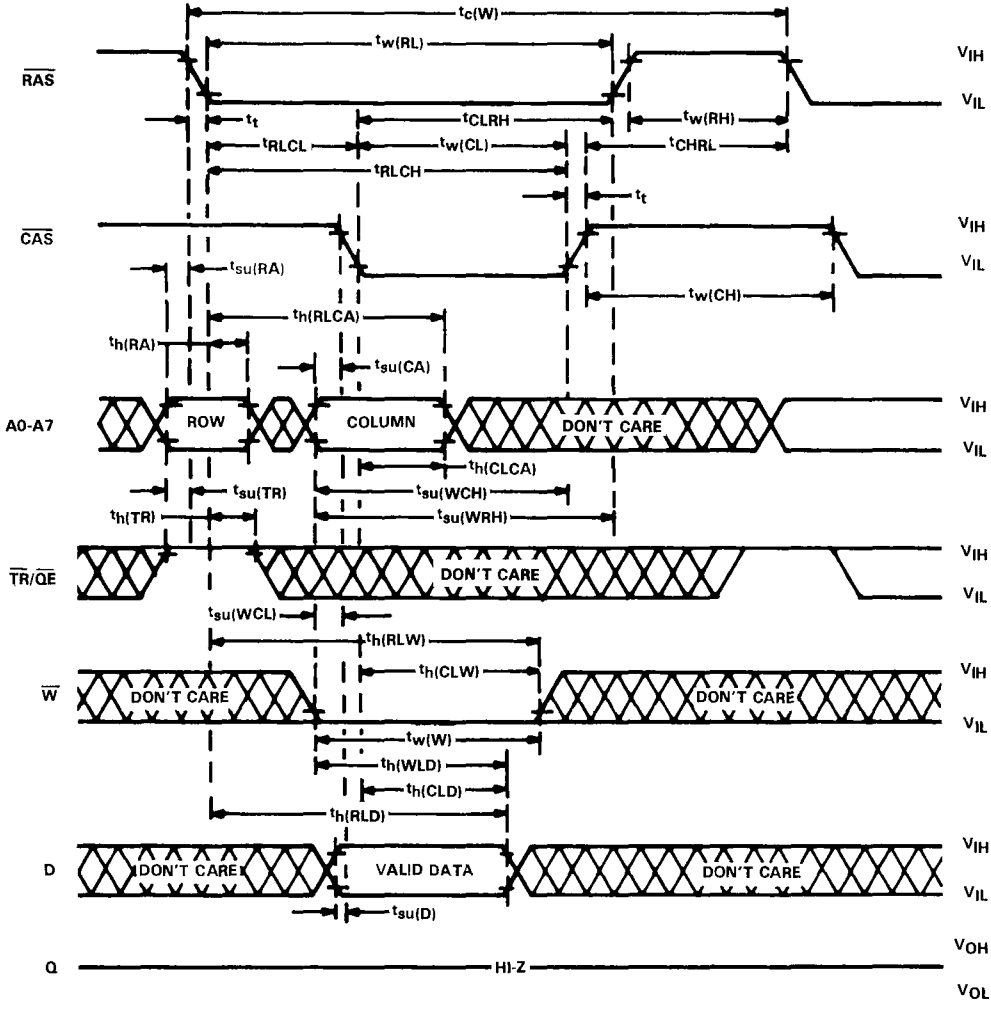
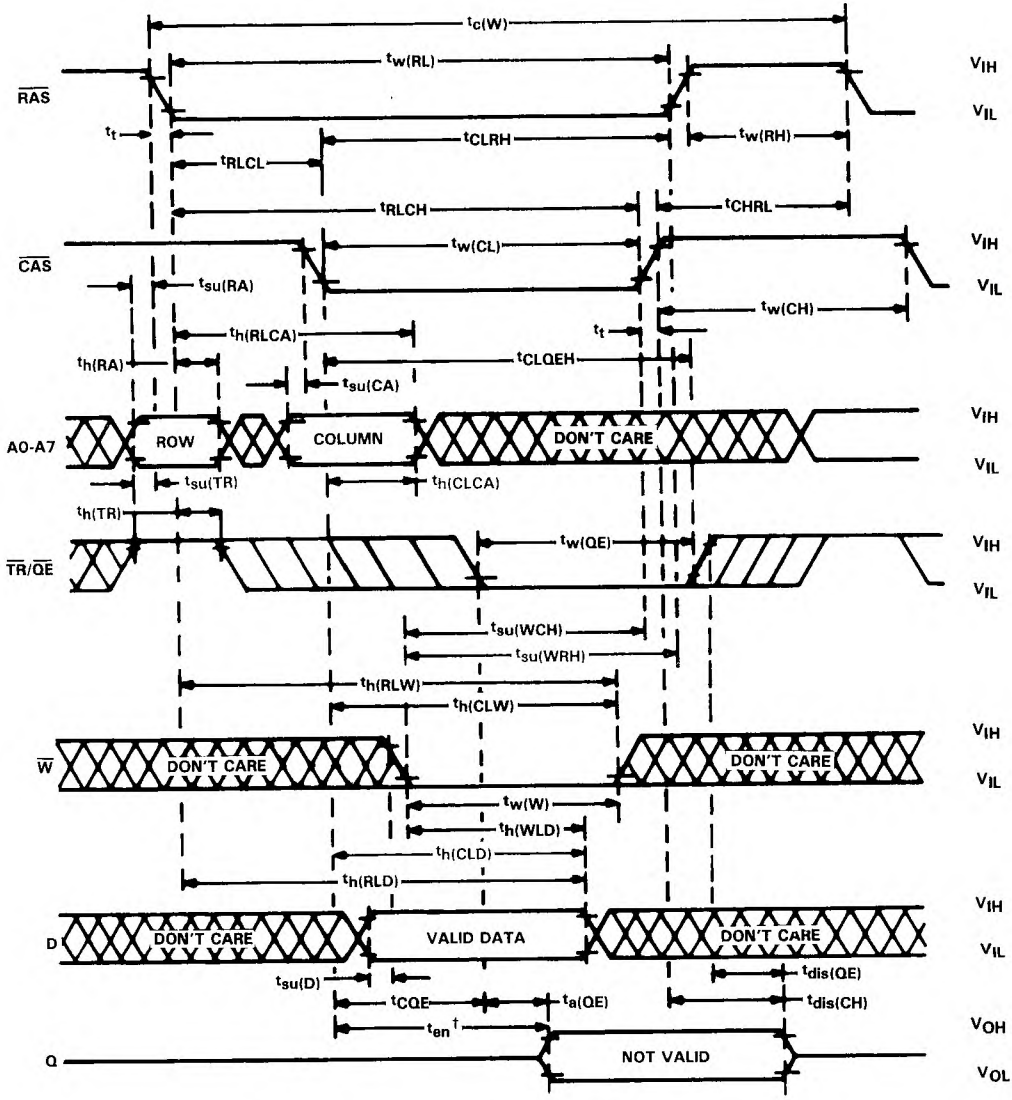
read cycle timing



early write cycle timing

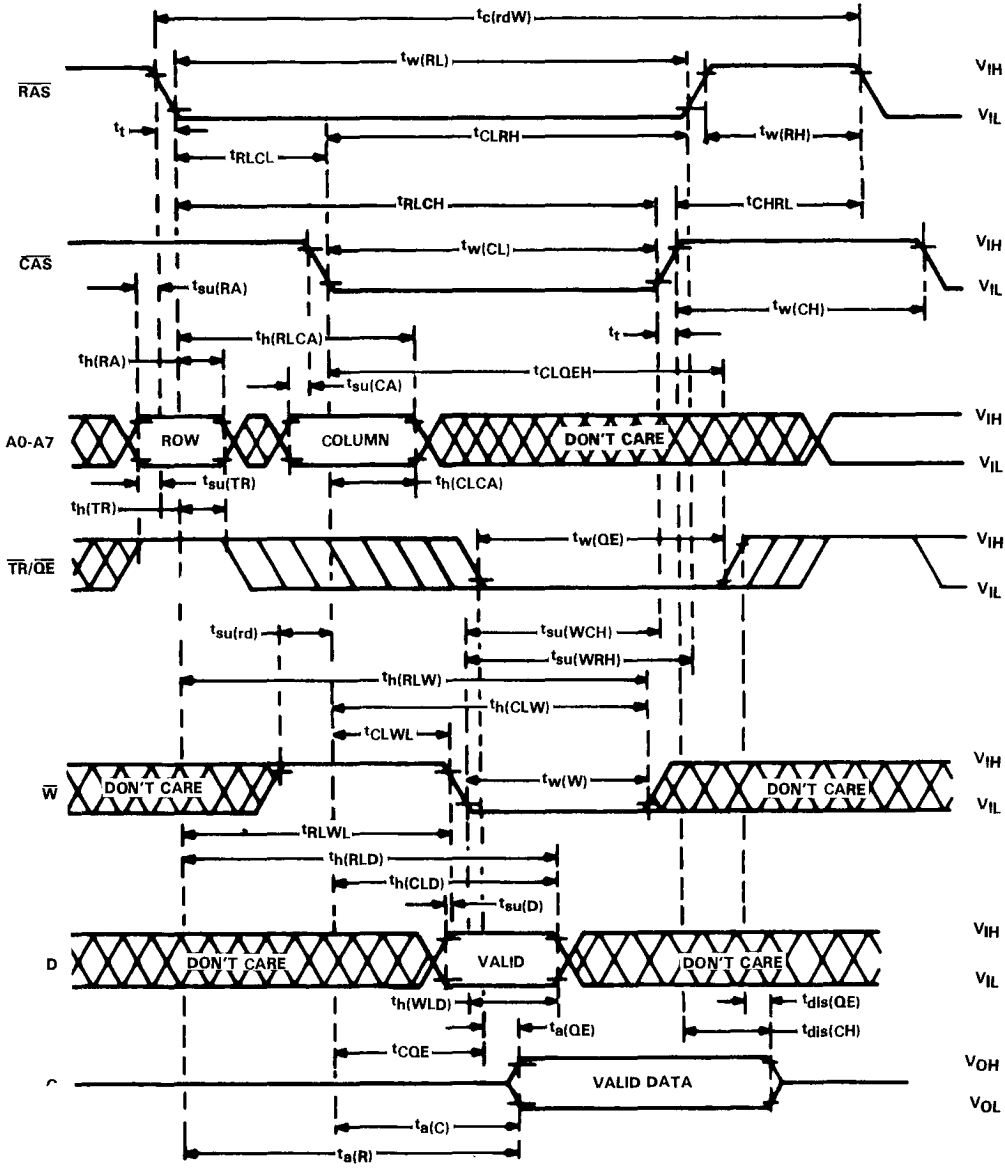


write cycle timing



†The enable time (t_{en}) for a write cycle is equal in duration to the access time from $\overline{CAS}$ ($t_{a(C)}$) in a read cycle; but the active levels at the output are invalid.

read-write/read-modify-write cycle timing



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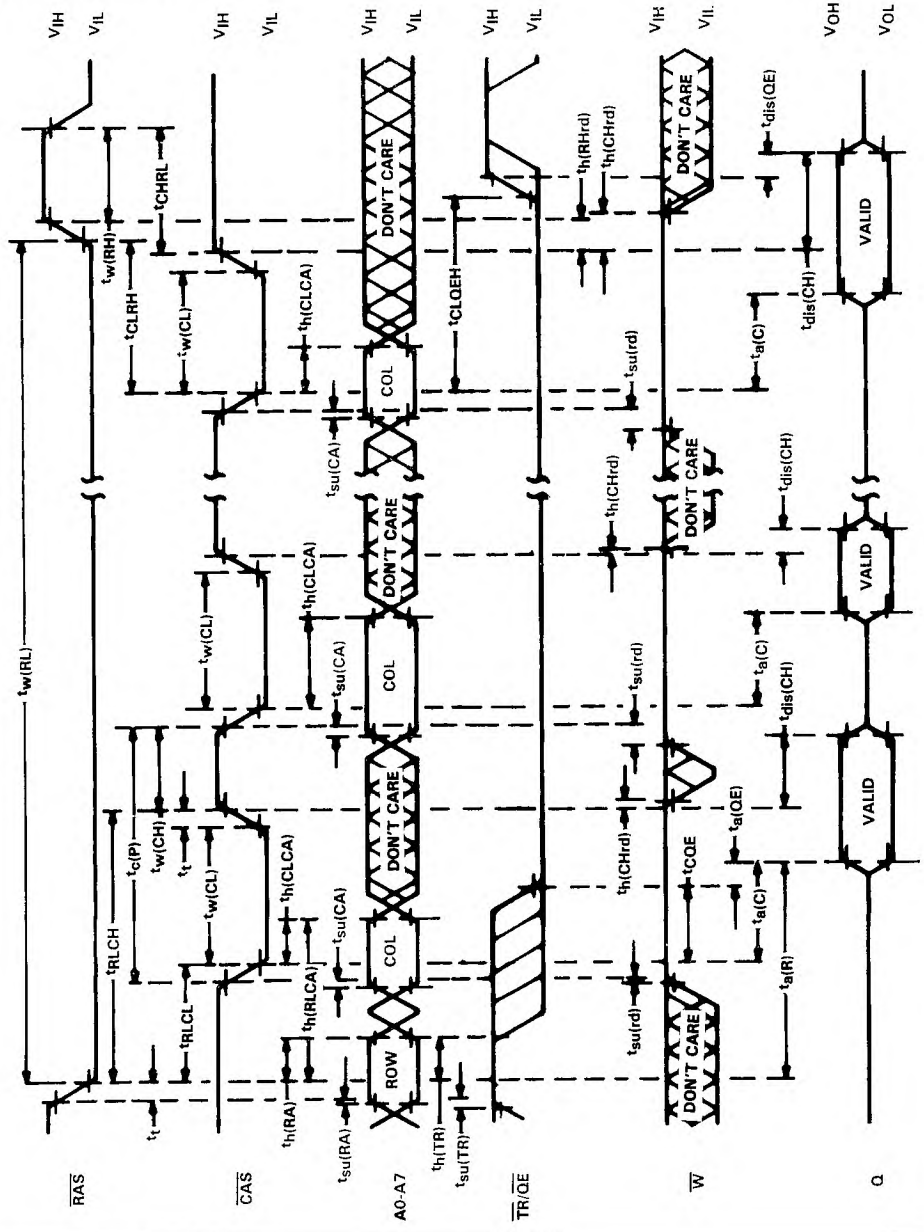
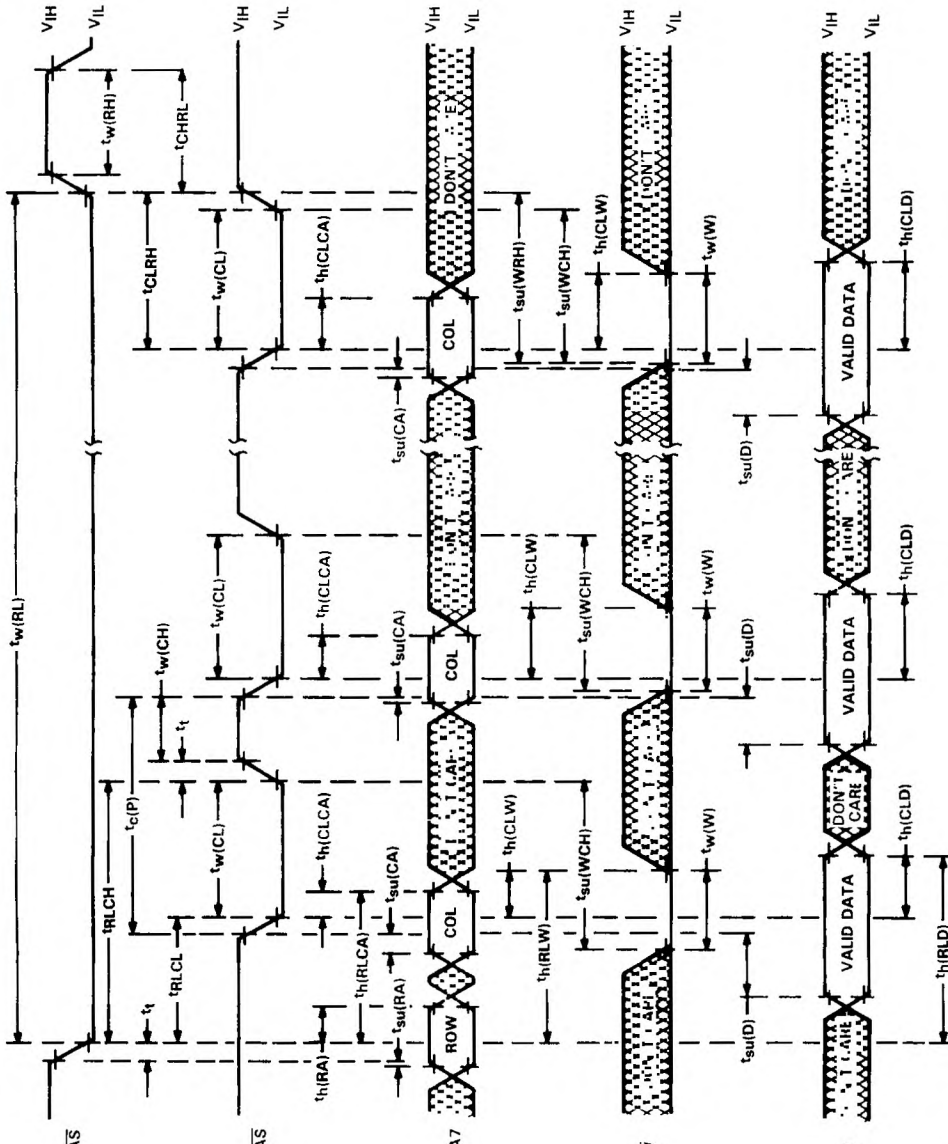
page-mode read cycle timing



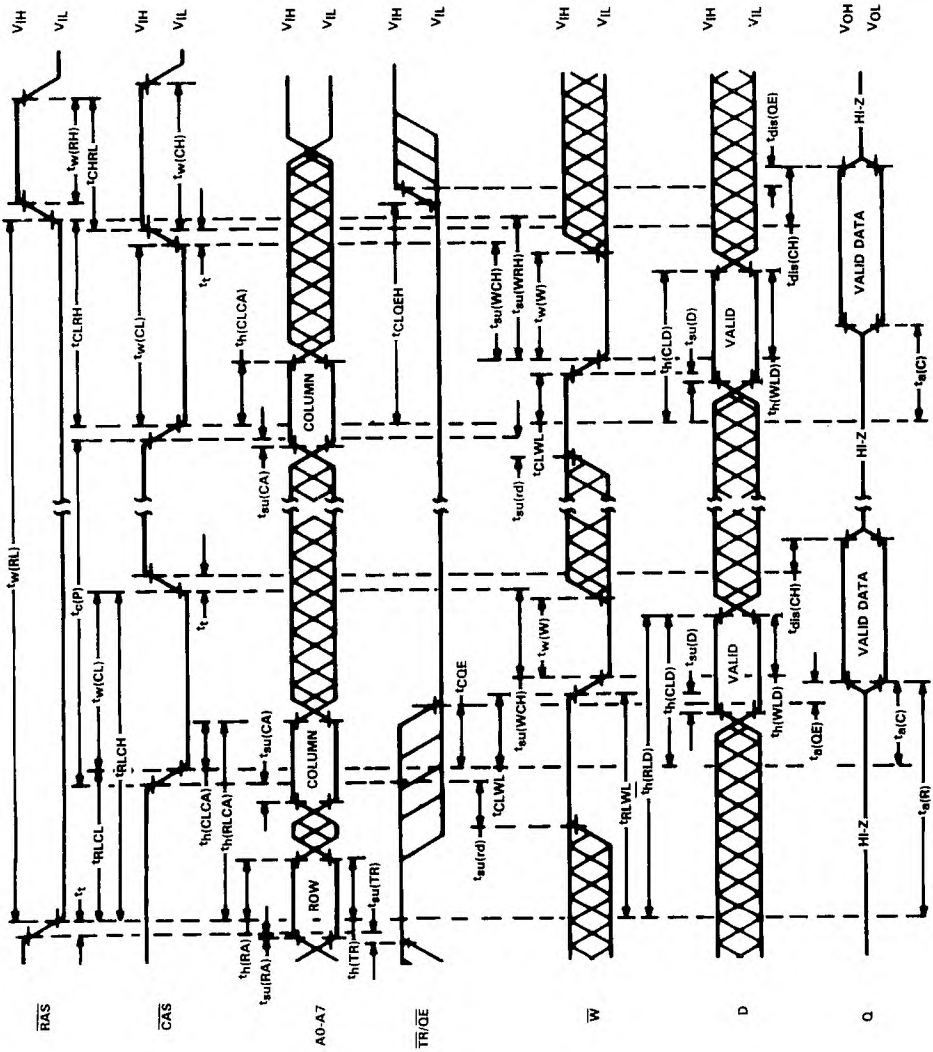
NOTES: 7. Timing is for non-multiplexed D, Q, and Address lines.
8. A write cycle or a read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

page-mode write cycle timing



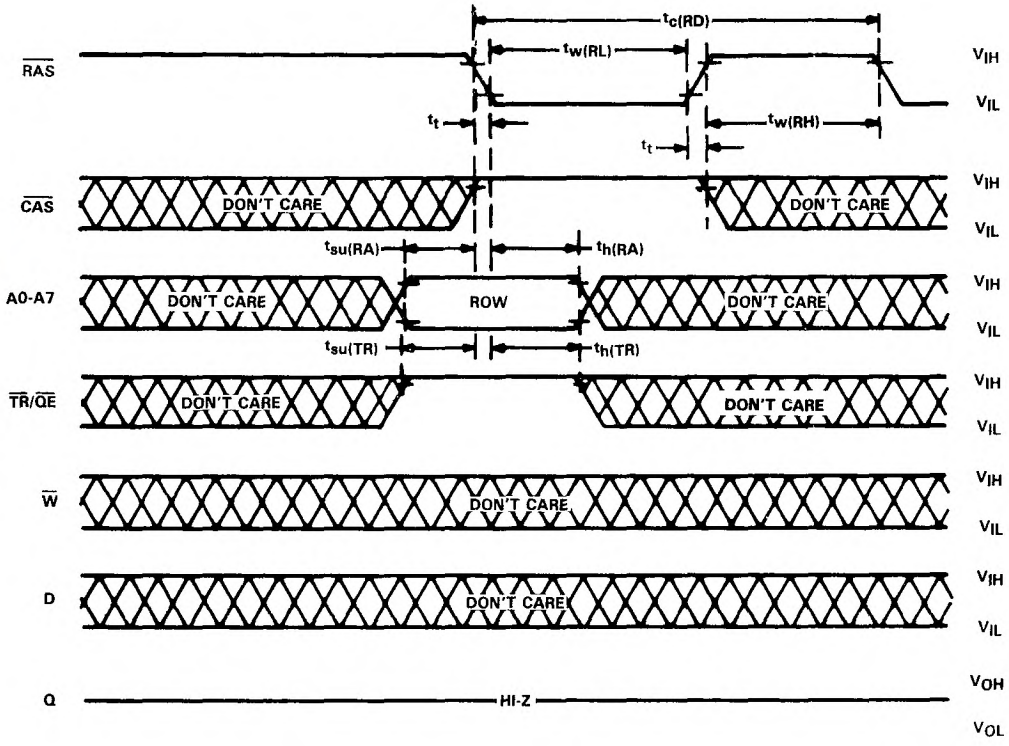
NOTES: 7. Timing is for non-multiplexed D, Q, and Address lines.
9. A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as the read and read-modify-write timing specifications are not violated.

page-mode read-modify-write cycle timing



NOTES: 7. Timing is for non-multiplexed D, Q, and Address lines.
10. A read cycle or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

$\overline{\text{RAS}}$-only refresh timing



TEXAS INSTRUMENTS
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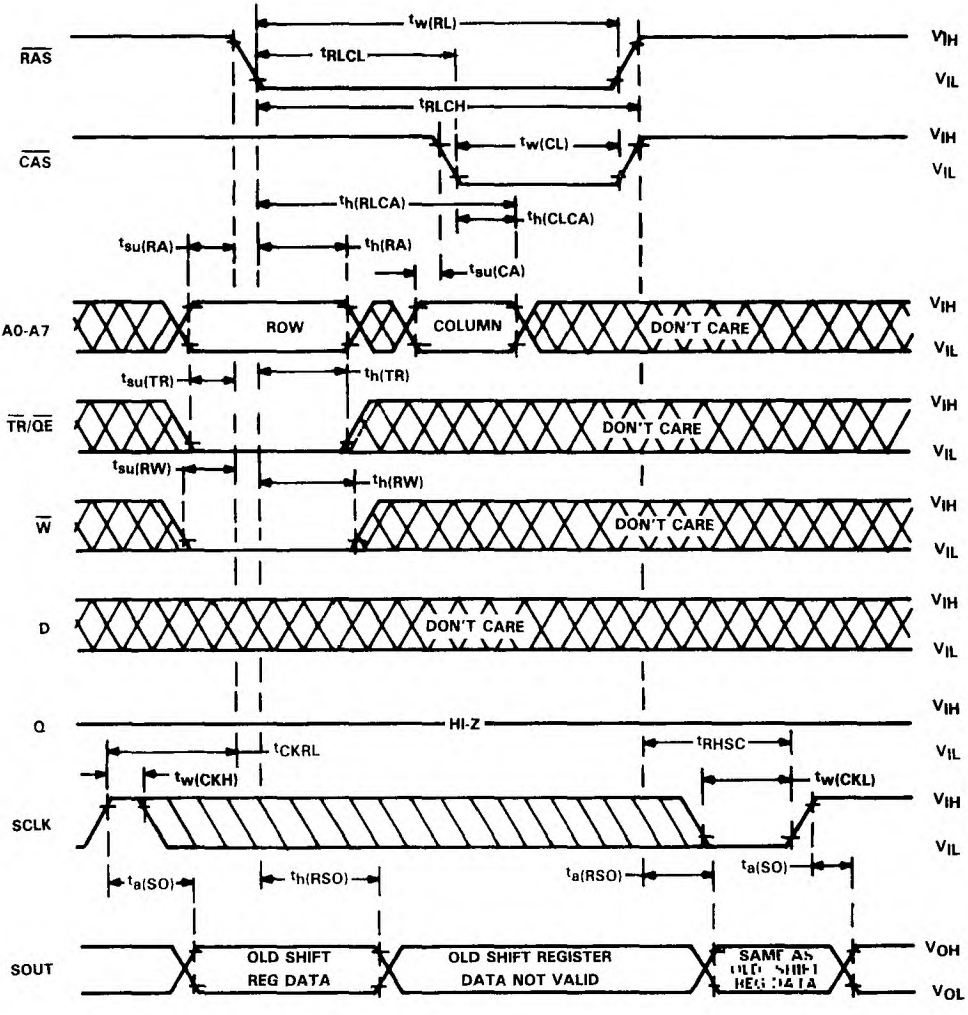
shift register to memory timing

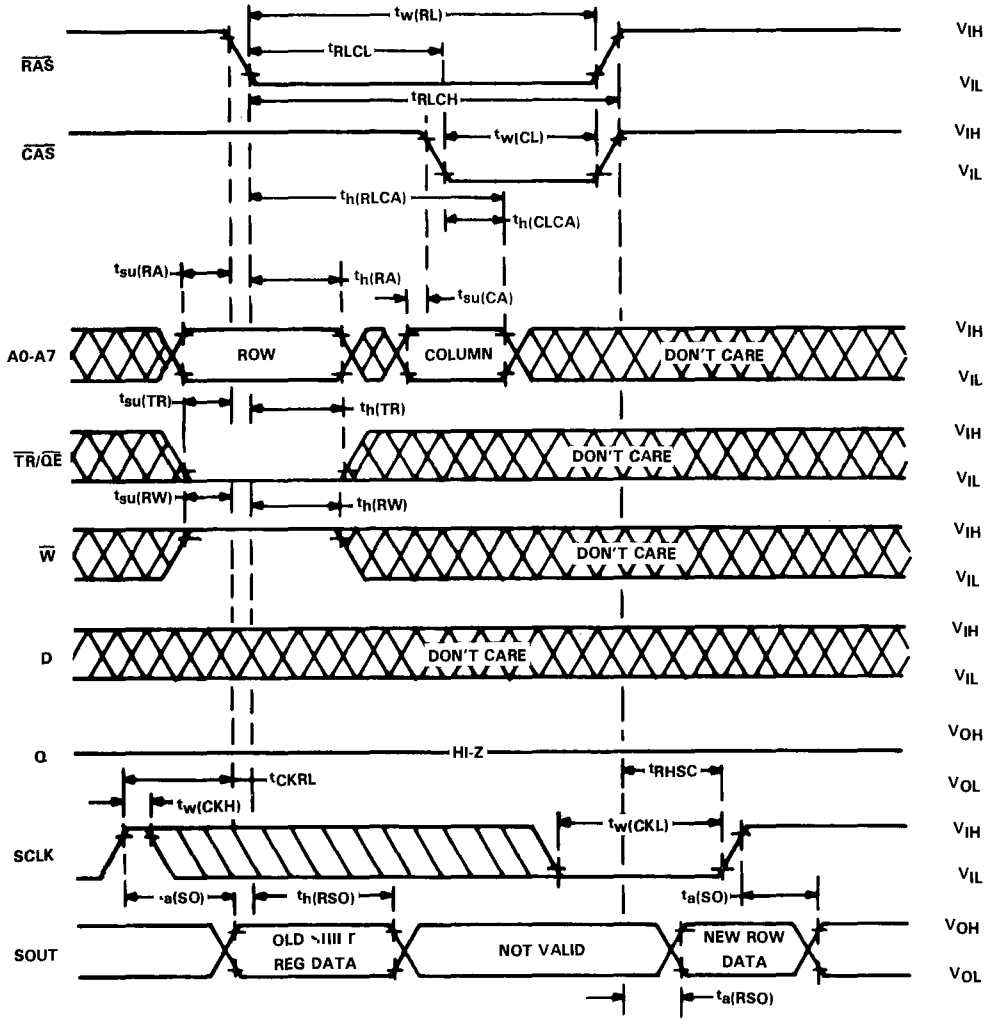


NOTES: 11. The shift register to memory cycle is used to transfer data from the shift register to the memory array. Every one of the 256 locations in the shift register is written into the 256 columns of the selected row. Note that the data that was in the shift register may have resulted, either from a serial shift in or from a parallel load of the shift register from one of the memory [illegible] rows.

12. [illegible] assumed low.

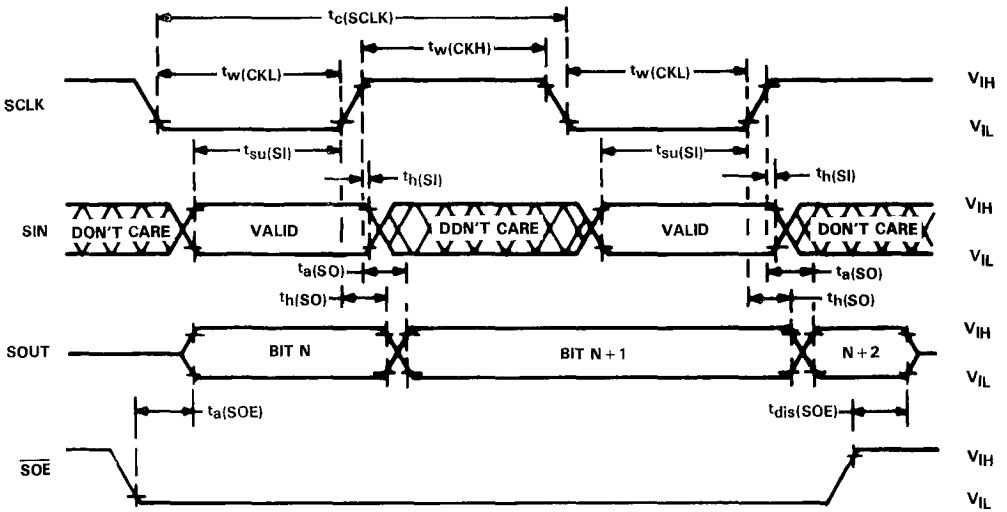
13. SCLK may be high or low during $t_{w(RL)}$.

memory to shift register timing



NOTES: 12. $\overline{SOE}$ assumed low.
13. SCLK may be high or low during $t_{w(RL)}$.
14. The memory to shift register cycle is used to load the shift register in parallel from the memory array. Every one of the 256 locations in the shift register are written into from the 256 columns of the selected row. Note that the data that is loaded into the shift register may be either shifted out or written back into another row.

serial data shift timing



NOTES: 15. When loading data into the shift register from the serial input in preparation for a shift register to memory transfer operation, the serial clock must be clocked an even number of times.

16. While shifting data through the serial shift register, the state of $\overline{TR}/\overline{QE}$ is a don't care as long as $\overline{TR}/\overline{QE}$ is held high when $\overline{RAS}$ goes low and $t_{su(TR)}$ and $t_{h(TR)}$ timings are observed. This requirement avoids the initiation of a register-to-memory or memory-to-register data transfer operation. The serial data transfer cycle is used to shift data in and/or out of the shift register.

shift register to memory multiple timing

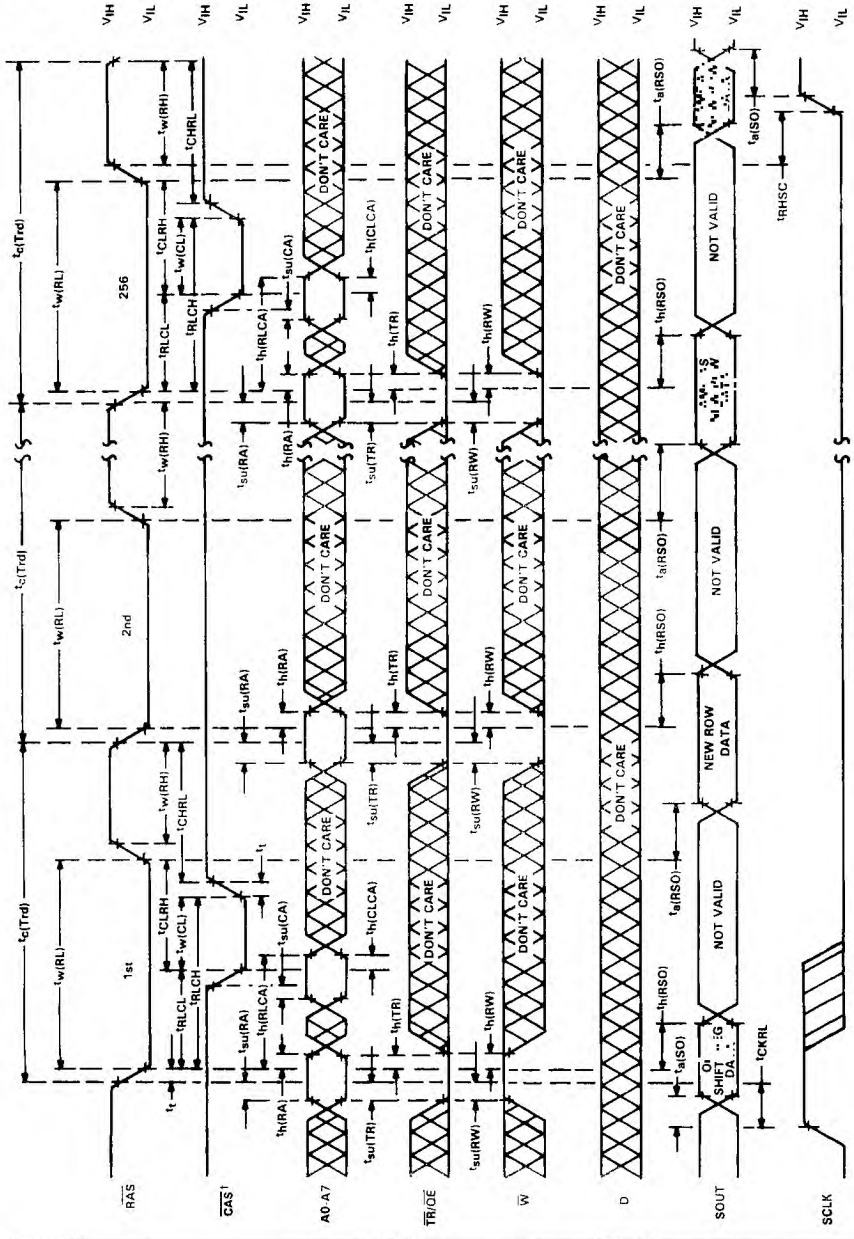
† $\overline{CAS}$ and re · address need not be supplied every cycle, only when it is desired to change or select a new register length.

NOTES: 12. assumed low.

17. The shift register to memory multiple cycle is used to write the shift register data to more than one row of the memory array. An application of this could be clearing all memory. To do this, the SIN line would be held at 0 to fill all locations in the shift register with 0's. The shift register would then be written into all 256 rows of the memory array in 256 cycles. The random output port Q will be in a high-impedance state as long as register transfer cycles are selected.

18. SCLK is a don't care except that no positive transitions on SCLK can occur for a period equal to t_{CKRL} prior to $\overline{RAS}$ falling with $\overline{TR}/\overline{OE}$ low.

memory to shift register to memory multiple timing



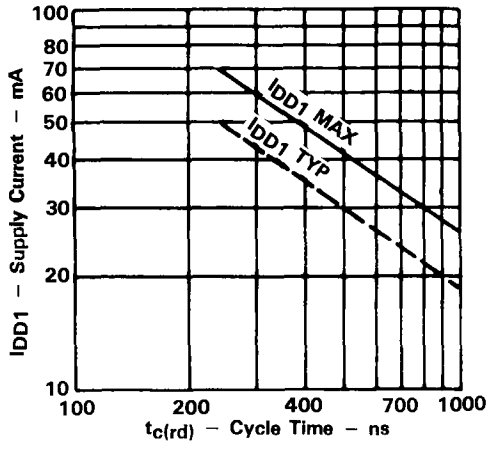
†$\overline{CAS}$ and register address need not be supplied every transfer cycle, only when it is desired to change from one register address to another.

NOTES: 12. $\overline{SOE}$ assumed low.

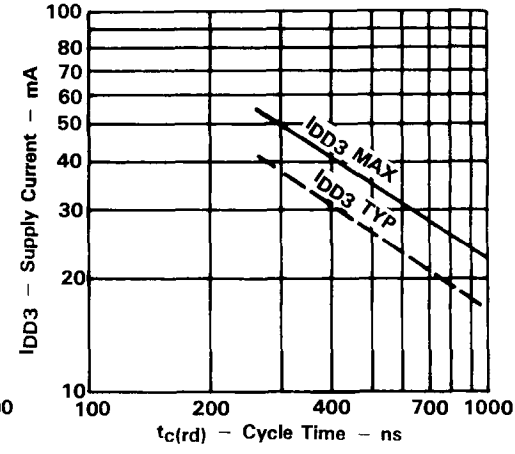
18. SCLK is a don't care except that no positive transitions on SCLK can occur for a period equal to t_{CKRL} prior to $\overline{RAS}$ falling with $\overline{TR}/\overline{OE}$ low.

19. The memory to shift register to memory multiple cycle is used to reorder the rows within the memory array itself. First, the data in a row is stored in the shift register and then it is written into other selected rows. The random output port Q will be in a high-impedance state as long as register transfer cycles are selected.

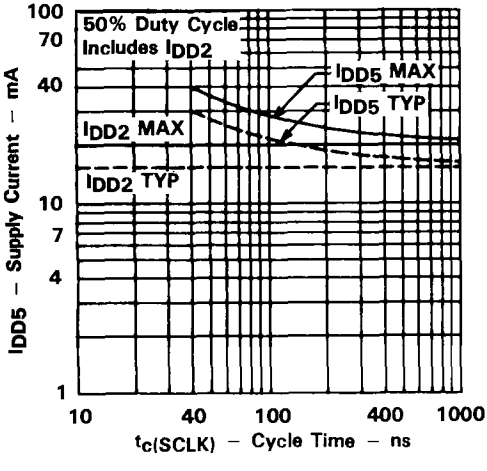
I_{DD1} vs CYCLE TIME



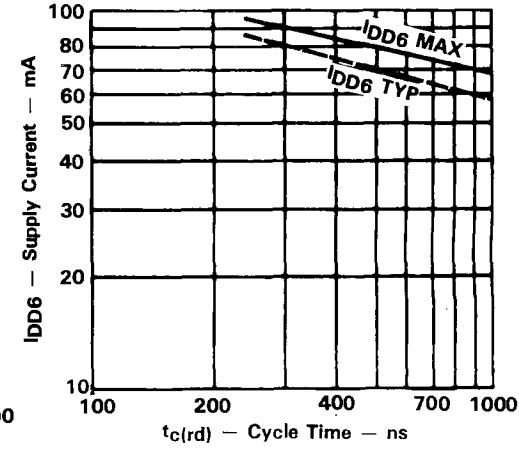
I_{DD3} vs CYCLE TIME



I_{DD5} vs CYCLE TIME



I_{DD6} vs CYCLE TIME



MAY 1985—REVISED NOVEMBER 1985

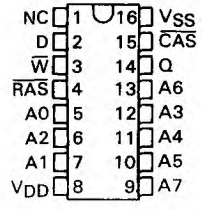
This Data Sheet Is Applicable to All TMS4164s Symbolized with Code "A" as Described on Page 4-57.

- **65,536 X 1 Organization**
- **Single 5-V Supply (10% Tolerance)**
- **JEDEC Standardized Pinout in Dual-in-Line Package**
- **Performance Ranges:**

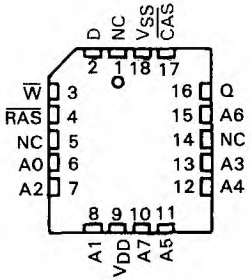
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY-WRITE CYCLE (MIN)
'4164-12	120 ns	70 ns	230 ns	255 ns
'4164-15	150 ns	85 ns	260 ns	290 ns
'4164-20	200 ns	135 ns	330 ns	345 ns

- **Upward Pin Compatible with TMS4116 (16K Dynamic RAM)**
- **First Military Version of 64K DRAM**
- **Also Available with MIL-STD-883B Processing and L(0°C to 70°C), E(−40°C to 85°C), S(−55°C to 100°C), or M(−55°C to 125°C) Temperature Ranges**
- **Operations of the TMS4164 Can Be Controlled by TI's TMS4500A and/or THCT4501 Dynamic RAM Controllers**
- **Long Refresh Period . . . 4 ms**
- **Low Refresh Overhead Time . . . As Low As 1.8% of Total Refresh Period**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Unlatched Output**
- **Common I/O Capability with Early Write Feature**
- **Page-Mode Operation for Faster Access**
- **Low Power Dissipation**
  - **Operating . . . 135 mW (Typ)**
  - **Standby . . . 17.5 mW (Typ)**
- **SMOS (Scaled-MOS) N-Channel Technology**

N PACKAGE
(TOP VIEW)



FP PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
NC	No Connection
Q	Data Out
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TMS4164 is a high-speed, 65,536-bit, dynamic random-access memory, organized as 65,536 words of one bit each. It employs state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon gate technology for very high performance combined with low cost and improved reliability.

The TMS4164 features $\overline{RAS}$ access times of 120 ns, 150 ns, and 200 ns maximum. Power dissipation is 135 mW typical operating and 17.5 mW typical standby.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility. Pin 1 has no internal connection to allow compatibility with other 64K RAMs that use this pin for an additional function.

The TMS4164 is offered in 16-pin dual-in-line plastic (N suffix) and 18-lead plastic chip carrier (FP suffix) packages. The dual-in-line plastic package is designed for insertion in mounting-hole rows on 7,62-mm (300-mil) centers. The TMS4164 is guaranteed for operation from 0°C to 70°C.

operation

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage cell locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (D)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In an early write cycle, the output is always in the high-impedance state. In a delayed-write or read-modify-write cycle, the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the ouput buffer is in the high-impedance state unless $\overline{CAS}$ is applied, The $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

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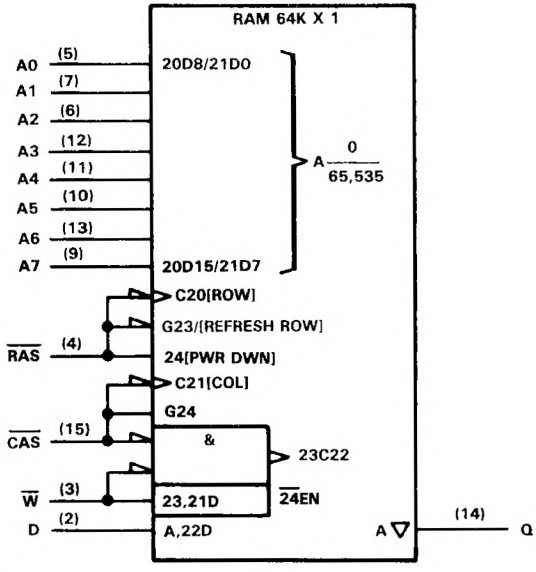
page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing random column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on a single RAM, the row address and $\overline{RAS}$ are applied to multiple 64K RAMs. $\overline{CAS}$ is then decoded to select the proper RAM.

power up

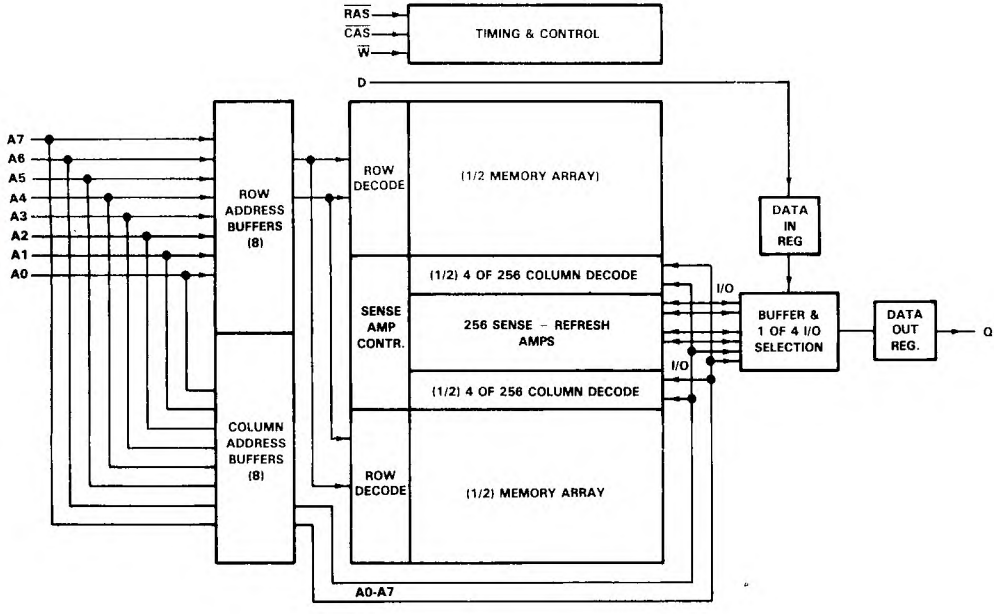
After power up, the power supply must remain at its steady-state value for 1 ms. In addition, $\overline{RAS}$ must remain high for 100 μs immediately prior to initialization. Initialization consists of performing eight RAS cycles before proper device operation is achieved.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the dual-in-line package.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage on any pin except V_{DD} and data out (see Note 1) . . . . . −1.5 V to 10 V
Voltage on V_{DD} supply and data out with respect to V_{SS} . . . . . −1 V to 6 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values in this data sheet are with respect to V_{SS}.
2. Additional information concerning the handling of ESD sensitive devices is available in a document entitled *"Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies"* in Section 12.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.5	5	5.5	V
V_{SS}	Supply voltage			0		V
V_{IH}		V_{DD} = 4.5 V	2.4		4.8	V
		V_{DD} = 5.5 V	2.4		6	
V_{IL}	Low-level input voltage (see Notes 3 and 4)		−0.6		0.8	V
T_A	Operating free-air temperature		0		70	°C

NOTES: 3. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

4. Due to input protection circuitry, the applied voltage may begin to clamp at −0.6 V. Test conditions must comprehend this occurrence. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.

4

Dynamic RAMs

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS4164-12			TMS4164-15			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I=0 V to 5.8 V, V_{DD}=5 V, All other pins = 0 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0.4 to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}‡	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		40	48		35	45	mA
I_{DD2}§	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		3.5	5		3.5	5	mA
I_{DD3}‡	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		28	40		25	37	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		28	40		25	37	mA

† All typical values are at T_A = 25°C and nominal supply voltages.
‡ Additional information on page 4-58.
§ V_{IL} > −0.6V. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS4164-20 MIN	TMS4164-20 TYP†	TMS4164-20 MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All other pins = 0 V			±10	μA
I_O	Output current (leakage)	V_O = 0.4 to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10	μA
I_{DD1}‡	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		27	37	mA
I_{DD2}§	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		3.5	5	mA
I_{DD3}‡	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, All outputs open		20	32	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, All outputs open		20	32	mA

†All typical values are at T_A = 25°C and nominal supply voltages.
‡Additional information on page 4-58.
§V_{IL} > −0.6V. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		TYP†	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs	4	5	pF
$C_{i(D)}$	Input capacitance, data input	4	5	pF
$C_{i(RC)}$	Input capacitance strobe inputs	6	8	pF
$C_{i(W)}$	Input capacitance, write enable input	6	8	pF
C_o	Output capacitance	5	6	pF

†All typical values are at T_A = 25°C and nominal supply voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS4164-12 MIN	TMS4164-12 MAX	TMS4164-15 MIN	TMS4164-15 MAX	UNIT
$t_{A(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		70		85	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	C_L = 100 pF, t_{RLCL} = MAX, Load = 2 Series 74 TTL gates	t_{RAC}		120		150	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	40	0	40	ns

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS4164-20		UNIT
				MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		135	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	C_L = 100 pF, t_{RLCL} = MAX, Load = 2 Series 74 TTL gates	t_{RAC}		200	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	50	ns

timing requirements over recommended supply voltage range and operating free-air temperature range (see Note 1)

		ALT. SYMBOL	TMS4164-12		TMS4164-15		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time	t_{PC}	130		145		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	230		260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	230		260		ns
$t_{c(rmw)}$	Read-write/read-modify-write cycle time	t_{RWC}	255		290		ns
$t_{w(CH)}$	Pulse duration, CAS high (precharge time)‡	t_{CP}	50		50		ns
$t_{w(CL)}$	Pulse duration, CAS low§	t_{CAS}	70	10,000	85	10,000	ns
$t_{w(RH)}$	Pulse duration, RAS high (precharge time)	t_{RP}	80		100		ns
$t_{w(RL)}$	Pulse duration, RAS low¶	t_{RAS}	120	10,000	150	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	40		45		ns
t_t	Transition times (rise and fall) for RAS and CAS	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	−5		−5		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCH)}$	Write-command setup time before CAS high	t_{CWL}	50		50		ns
$t_{su(WRH)}$	Write-command setup time before RAS high	t_{RWL}	50		50		ns
$t_{h(CLCA)}$	Column-address hold time after CAS low	t_{CAH}	40		45		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		20		ns
$t_{h(RLCA)}$	Column-address hold time after RAS low	t_{AR}	85		95		ns
$t_{h(CLD)}$	Data hold time after CAS low	t_{DHC}	40		45		ns
$t_{h(RLD)}$	Data hold time after RAS low	t_{DHR}	85		95		ns
$t_{h(WLD)}$	Data hold time after W low	t_{DHW}	40		45		ns
$t_{h(CHrd)}$	Read-command hold time after CAS high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read-command hold time after RAS high	t_{RRH}	5		5		ns
$t_{h(CLW)}$	Write-command hold time after CAS low	t_{WCH}	40		45		ns
$t_{h(RLW)}$	Write-command hold time after RAS low	t_{WCR}	85		95		ns
t_{RLCH}	Delay time, RAS low to CAS high	t_{CSH}	120		150		ns
t_{CHRL}	Delay time, CAS high to RAS low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, CAS low to RAS high	t_{RSH}	70		85		ns
t_{CLWL}	Delay time, CAS low to W low (read-modify-write cycle only)	t_{CWD}	40		60		ns
t_{RLCL}	Delay time, RAS low to CAS low (maximum value specified only to guarantee access time)	t_{RCD}	15	50	20	65	ns
t_{RLWL}	Delay time, RAS low to W low (read-modify-write cycle only)	t_{RWD}	110		120		ns
t_{WLCL}	Delay time, W low to CAS low (early write cycle)	t_{WCS}	−5		−5		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

NOTE 1: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

† All cycle times assume t_t = 5 ns.

‡ Page mode only.

§ In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional CAS low time ($t_{w(CL)}$). This applies to page-mode read-modify-write also.

¶ In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional RAS low time ($t_{w(RL)}$).

timing requirements over recommended supply voltage range and operating free-air temperature range (see Note 1)

		ALT. SYMBOL	TMS4164-20 MIN	TMS4164-20 MAX	UNIT
$t_{c(P)}$	Page-mode cycle time	t_{PC}	225		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	330		ns
$t_{c(W)}$	Write cycle time	t_{WC}	330		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	345		ns
$t_{w(CH)}$	Pulse duration, CAS high (precharge time)‡	t_{CP}	80		ns
$t_{w(CL)}$	Pulse duration, CAS low§	t_{CAS}	100	10,000	ns
$t_{w(RH)}$	Pulse duration, RAS high (precharge time)	t_{RP}	100		ns
$t_{w(RL)}$	Pulse duration, RAS low¶	t_{RAS}	200	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	55		ns
t_t	Transition times (rise and fall) for RAS and CAS	t_T	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	−5		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		ns
$t_{su(WCH)}$	Write-command setup time before CAS high	t_{CWL}	60		ns
$t_{su(WRH)}$	Write-command setup time before RAS high	t_{RWL}	60		ns
$t_{h(CLCA)}$	Column-address hold time after CAS low	t_{CAH}	55		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	25		ns
$t_{h(RLCA)}$	Column-address hold time after RAS low	t_{AR}	100		ns
$t_{h(CLD)}$	Data hold time after CAS low	t_{DHC}	55		ns
$t_{h(RLD)}$	Data hold time after RAS low	t_{DHR}	145		ns
$t_{h(WLD)}$	Data hold time after W low	t_{DHW}	55		ns
$t_{h(CHrd)}$	Read-command hold time after CAS high	t_{RCH}	0		ns
$t_{h(RHrd)}$	Read-command hold time after RAS high	t_{RRH}	5		ns
$t_{h(CLW)}$	Write-command hold time after CAS low	t_{WCH}	55		ns
$t_{h(RLW)}$	Write-command hold time after RAS low	t_{WCR}	145		ns
t_{RLCH}	Delay time, RAS low to CAS high	t_{CSH}	200		ns
t_{CHRL}	Delay time, CAS high to RAS low	t_{CRP}	0		ns
t_{CLRH}	Delay time, CAS low to RAS high	t_{RSH}	135		ns
t_{CLWL}	Delay time, CAS low to W low (read-modify-write cycle only)	t_{CWD}	65		ns
t_{RLCL}	Delay time, RAS low to CAS low (maximum value specified only to guarantee access time)	t_{RCD}	25	65	ns
t_{RLWL}	Delay time, RAS low to W low (read-modify-write cycle only)	t_{RWD}	130		ns
t_{WLCL}	Delay time, W low to CAS low (early write cycle)	t_{WCS}	−5		ns
t_{rf}	Refresh time interval	t_{REF}		4	ms

NOTE 1: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

† All cycle times assume t_t = 5 ns.

‡ Page mode only.

§ In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional CAS low time ($t_{w(CL)}$). This applies to page-mode read-modify-write also.

¶ In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional RAS low time ($t_{w(RL)}$).

PARAMETER MEASUREMENT INFORMATION

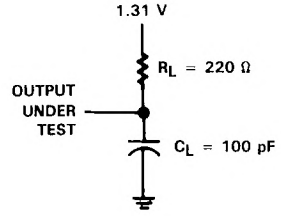
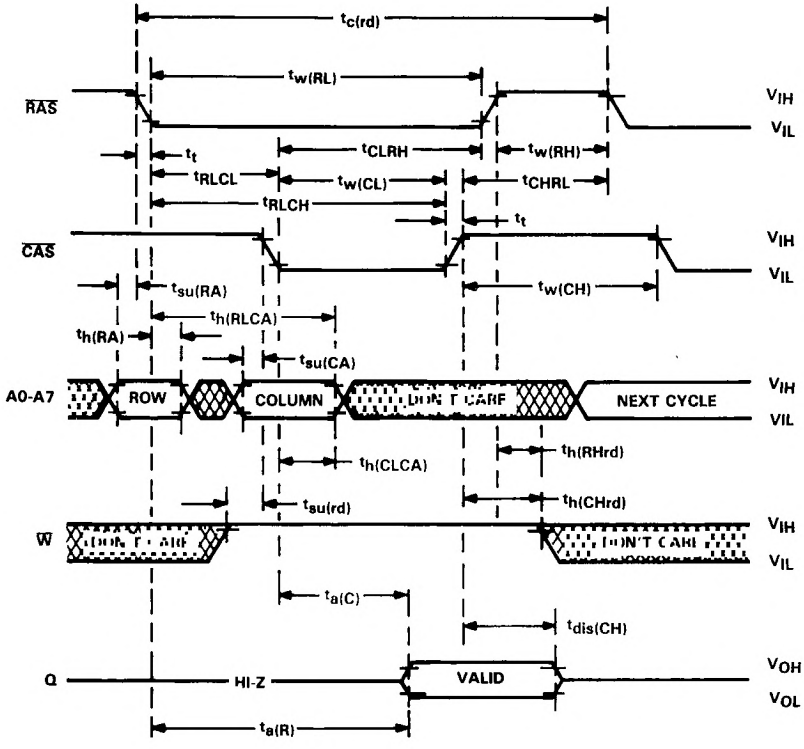


FIGURE 1. LOAD CIRCUIT

read cycle timing



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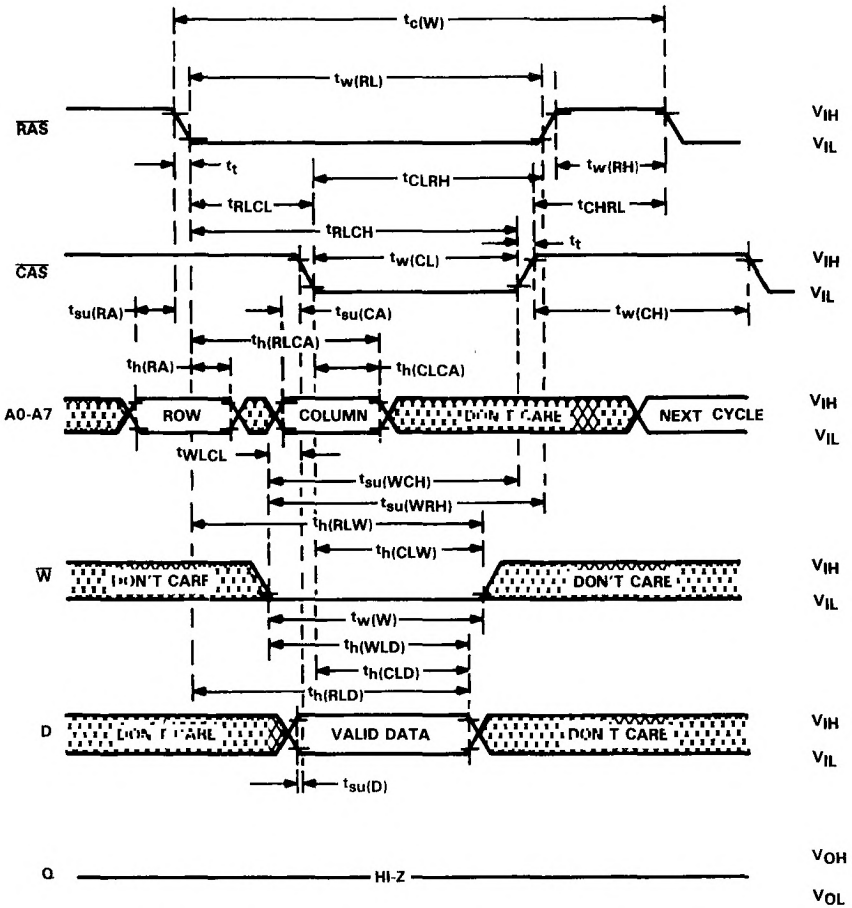
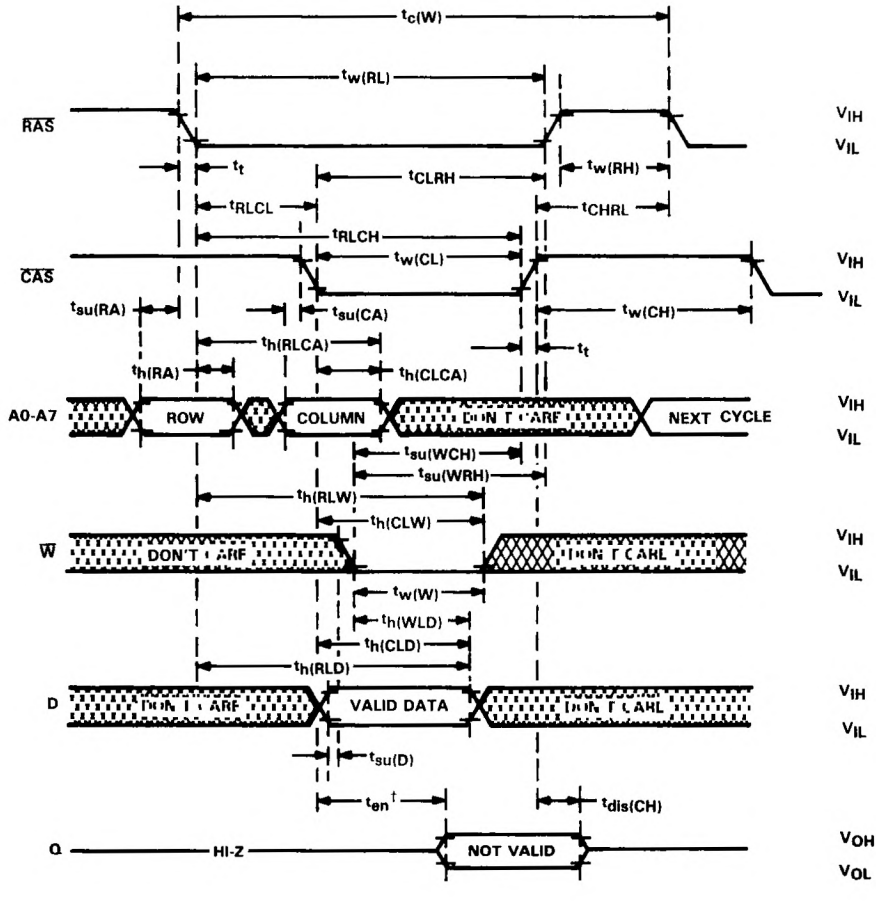
early write cycle timing

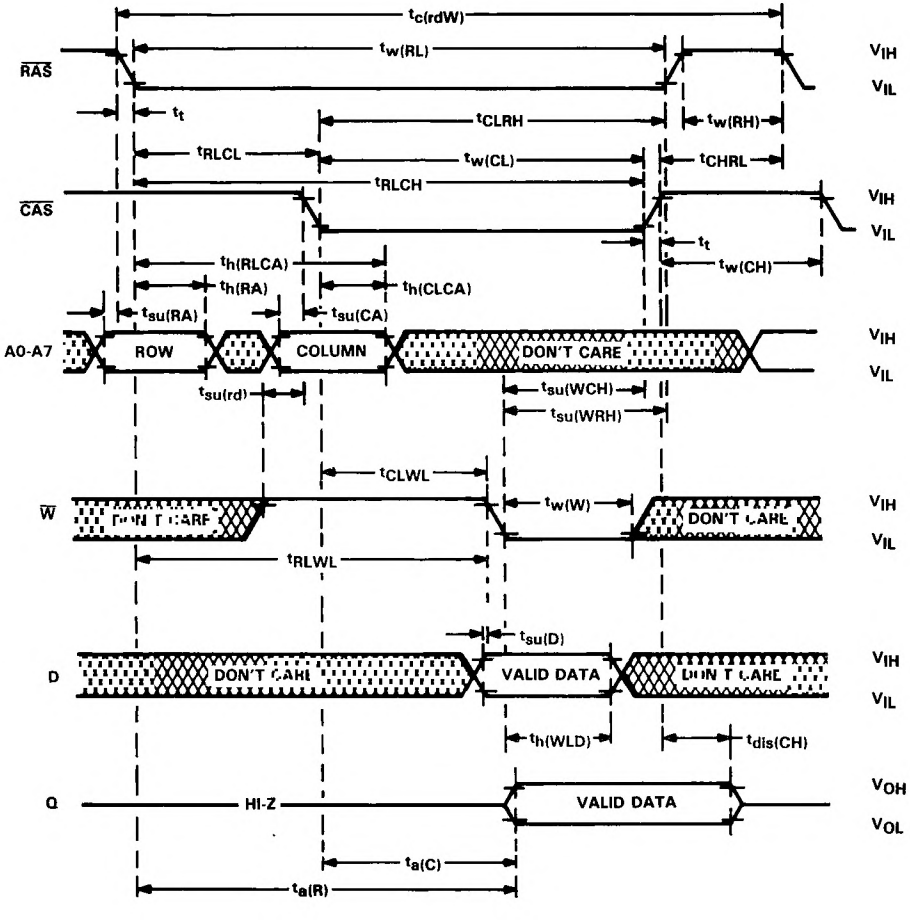


write cycle timing

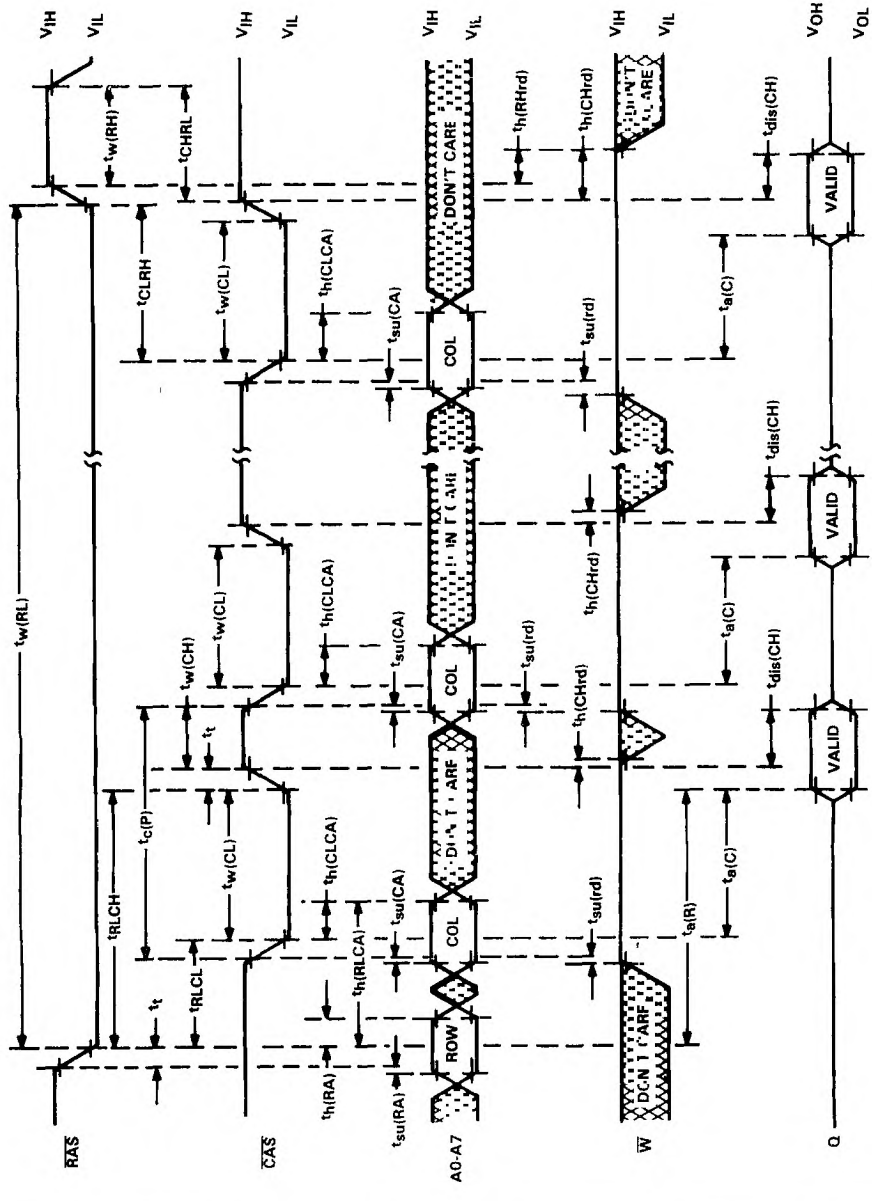


† The enable time (t_{en}) for a write cycle is equal in duration to the access time from $\overline{CAS}$ ($t_{a(C)}$) in a read cycle; but the active levels at the output are invalid.

read-modify-write cycle timing

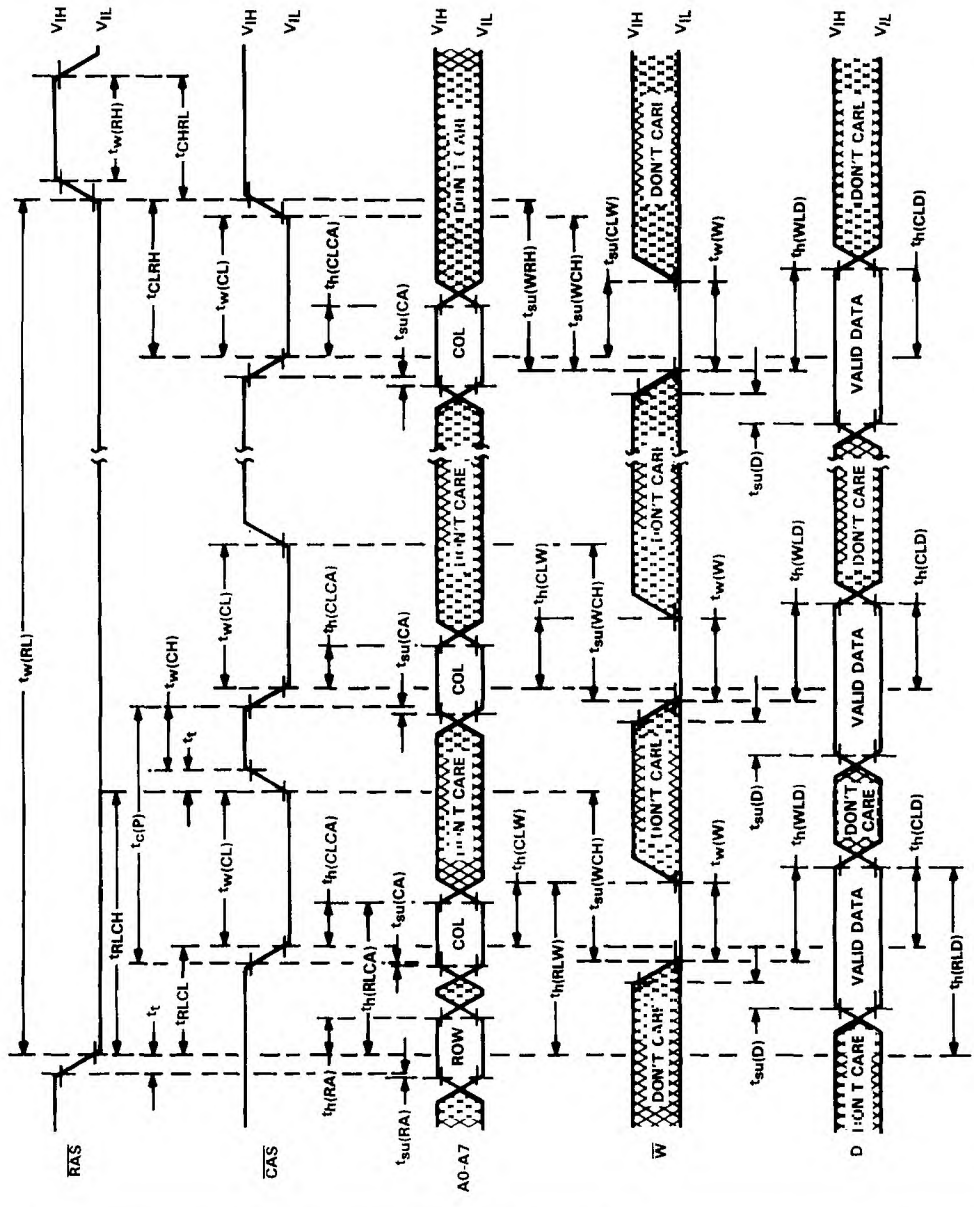


page-mode read cycle timing



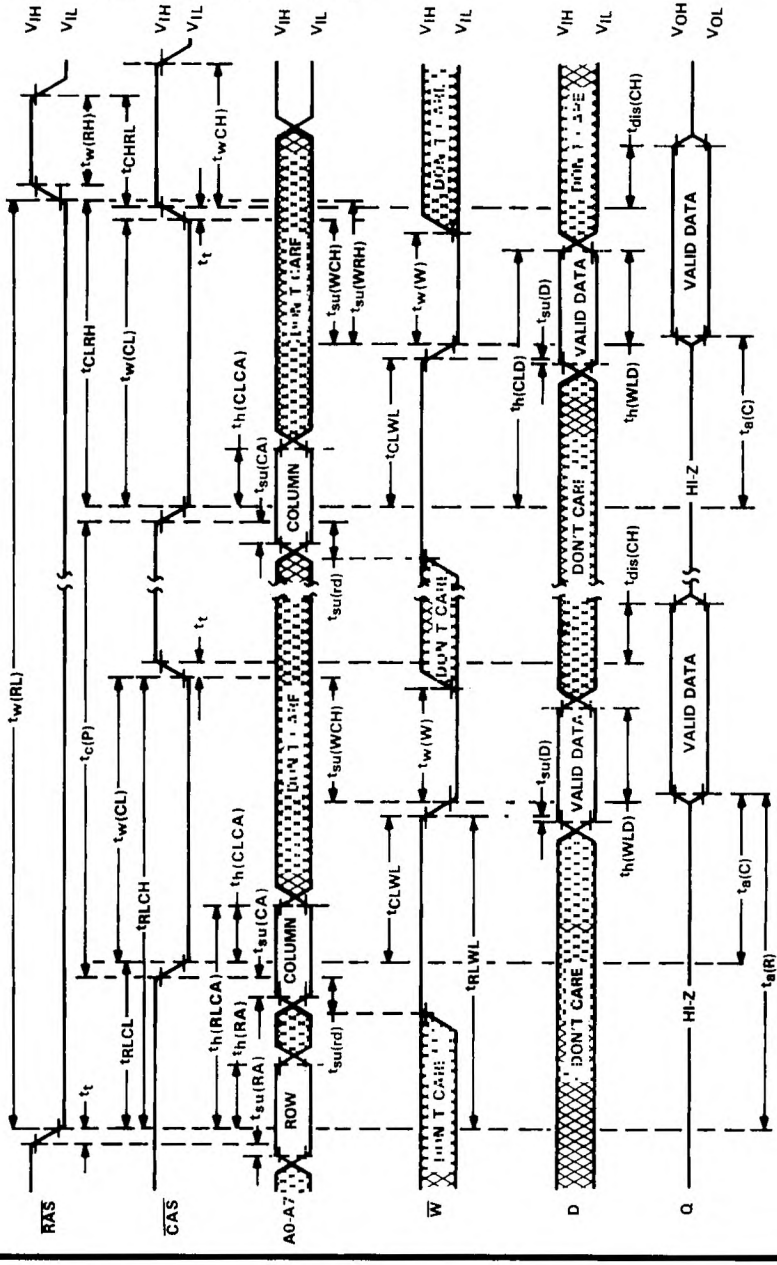
NOTE 2: A write cycle or a read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

page-mode write cycle timing



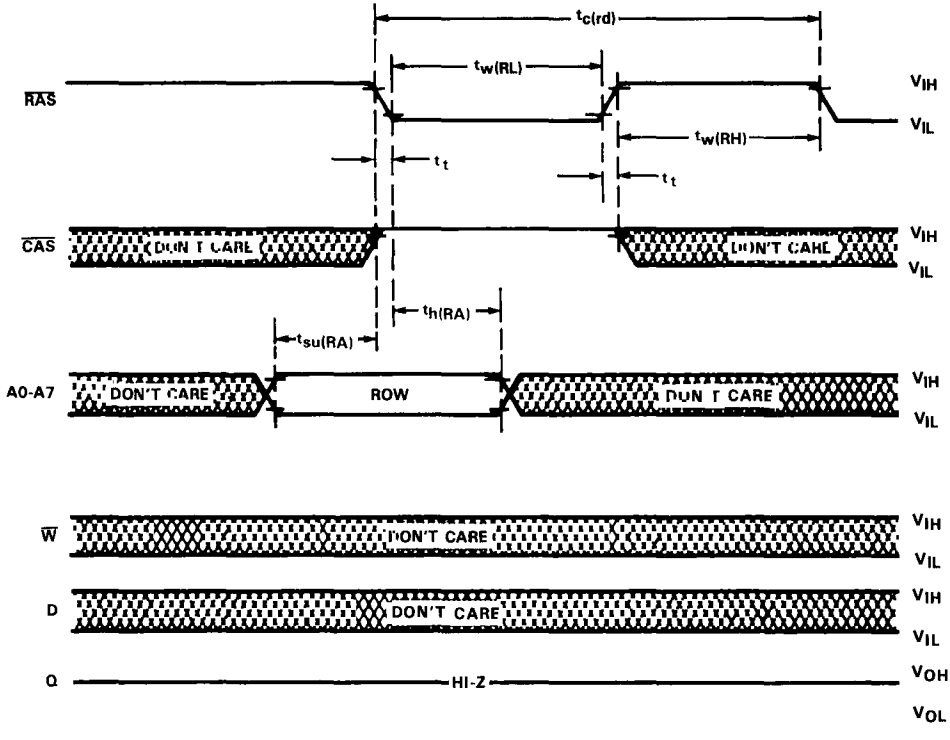
NOTE 3: A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as the read and read-modify-write timing specifications are not violated.

page-mode read-modify-write cycle timing



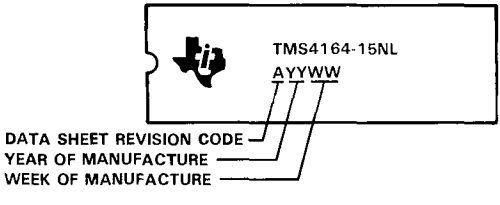
NOTE 4: A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

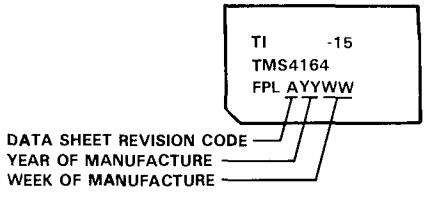
$\overline{\text{RAS}}$-only refresh timing



device symbolization

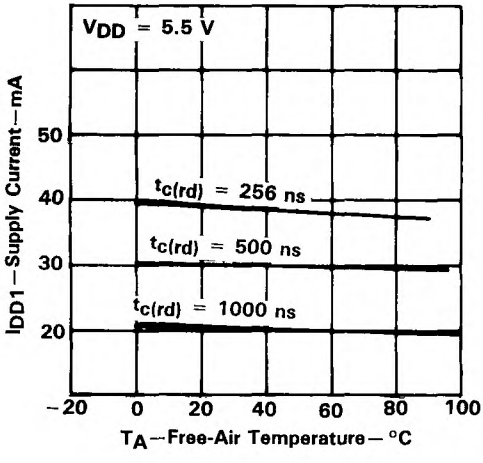
This data sheet is applicable to all TI TMS4164 Dynamic RAMs with the code "A" to the left of the date code as shown below:



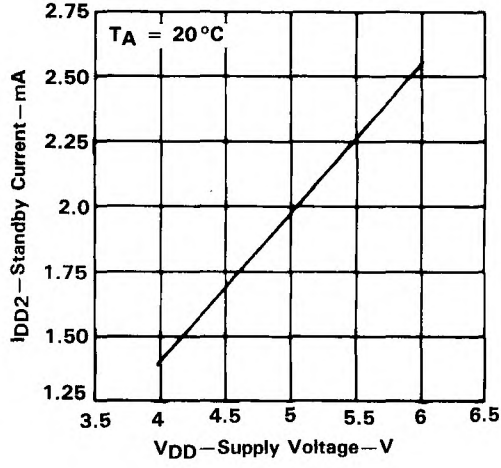


TYPICAL CHARACTERISTICS

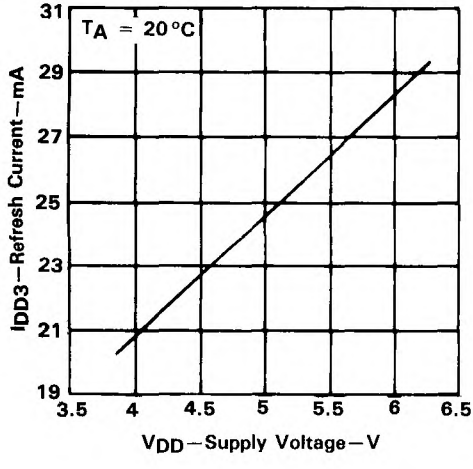
TYPICAL SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



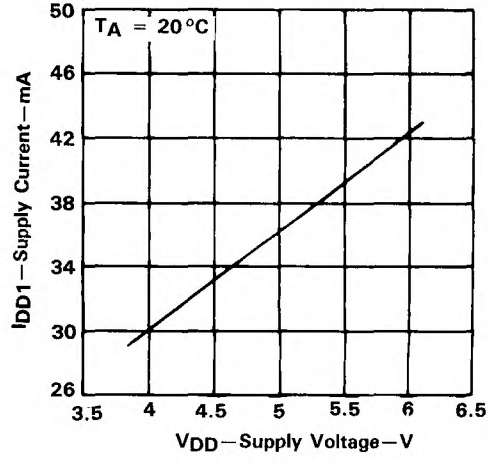
TYPICAL SUPPLY CURRENT
vs
SUPPLY VOLTAGE



TYPICAL SUPPLY CURRENT
vs
SUPPLY VOLTAGE



TYPICAL SUPPLY CURRENT
vs
SUPPLY VOLTAGE



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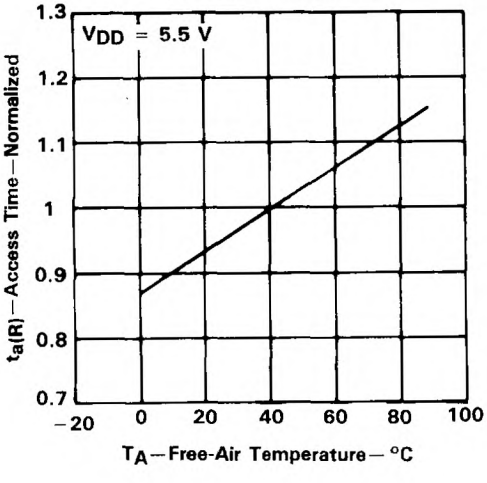
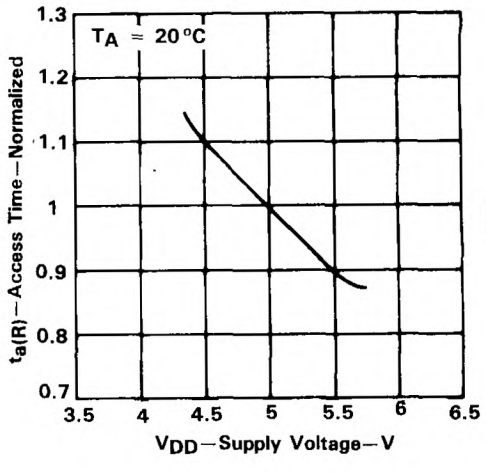
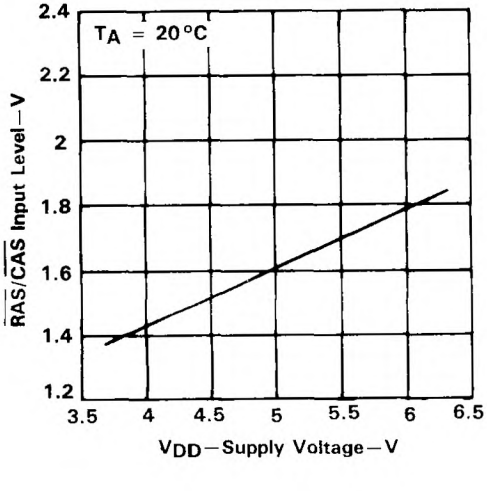
ACCESS TIME
vs
FREE-AIR TEMPERATURE



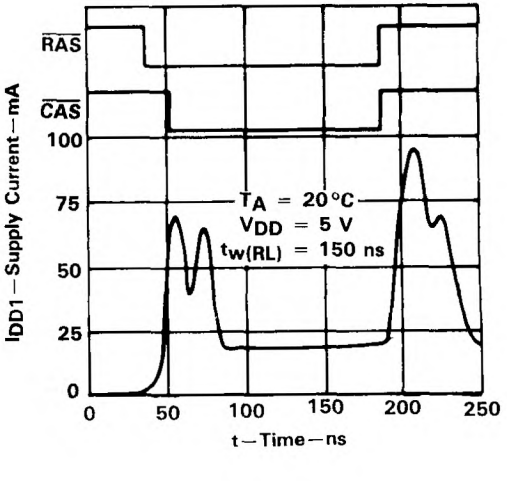
ACCESS TIME
vs
SUPPLY VOLTAGE



$\overline{RAS}/\overline{CAS}$ INPUT LEVEL
vs
SUPPLY VOLTAGE



AVERAGE CURRENT
DURING AN OPERATING CYCLE



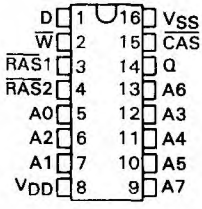
APRIL 1985 – REVISED NOVEMBER 1985

- 2 X 65,536 X 1 Organization
- Single 5-V Supply (10% Tolerance)
- Operating Free-Air Temperature . . . 0°C to 70°C
- Long Refresh Period . . . 4 ms
- Low Refresh Overhead Time . . . As Low As 1.8% of Total Refresh Period
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Unlatched Output
- Common I/O Capability with "Early Write" Feature
- Page-Mode Operation for Faster Access
- Low Power Dissipation
  - Operating . . . 193 mW (Typ)
  - Standby . . . 35 mW (Typ)
- Max Access/Min Cycle Times:

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY-WRITE CYCLE (MIN)
TMS41128B-15	150 ns	85 ns	260 ns	315 ns

- SMOS (Scaled-MOS) N-Channel Technology

16-PIN PLASTIC DUAL-IN-LINE STACKED PACKAGES †
(TOP VIEW)



† $\overline{RAS}1$ (pin 3) selects the lower DRAM, and pin 3 on the upper DRAM is a no connect. $\overline{RAS}2$ (pin 4) selects the upper DRAM, and pin 4 on the lower DRAM is a no connect.

PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
Q	Data Out
$\overline{RAS}1$, $\overline{RAS}2$	Row-Address Strobes
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TMS41128B consists of two high-speed, 65,536-bit, dynamic random-access memories that are separately packaged. These DRAMs are electrically similar to TMS4164s; however, the pin out is different. The two packages are permanently connected, pin for pin, one on top of the other. The result is a 16-pin memory device organized as 131,072 words of one bit each with essentially the same characteristics of the TMS4164 NMOS dynamic RAM.

A logic low on the $\overline{RAS}1$ input selects the lower DRAM; a logic low on the $\overline{RAS}2$ input selects the upper DRAM.

The TMS41128B-15 features a $\overline{RAS}$ access time of 150 ns. Power dissipation is 193 mW typical operating, 35 mW typical standby.

Refresh period is extended to 4 ms, and during this period each of the 256 rows must be strobed with $\overline{RAS}1$ and $\overline{RAS}2$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clock, are compatible with Series 74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS41128B is offered in 16-pin plastic dual-in-line stacked packages and is guaranteed for operation from 0°C to 70°C. This package is designed for insertion in mounting-hole rows on 300-mil (7,62-mm) centers.

operation

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage cell locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}1$ or $\overline{RAS}2$). Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}1$, $\overline{RAS}2$, and $\overline{CAS}$. $\overline{RAS}1$ and $\overline{RAS}2$ are similar to a chip enable in that they activate the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers. When $\overline{CAS}$ is applied to the device, only one of the $\overline{RAS}$ signals (either $\overline{RAS}1$ or $\overline{RAS}2$) must be applied to select either the lower DRAM or the upper DRAM. When a $\overline{RAS}$-only refresh is performed ($\overline{CAS}$ logic high), both $\overline{RAS}1$ and $\overline{RAS}2$ may be applied simultaneously.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (D)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In an early write cycle, the output is always in the high-impedance state. In a delayed-write or read-modify-write cycle, the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least every 4 ms on both DRAMs to retain data. Since the output buffer is in the high-impedance state unless $\overline{CAS}$ is applied, The $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with both $\overline{RAS}1$ and $\overline{RAS}2$ causes all bits in each row to be refreshed. $\overline{CAS}$ must remain high (inactive) for this refresh sequence.

page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on a single RAM, the row address and $\overline{RAS}$ are applied to multiple 64K RAMs. $\overline{CAS}$ is then decoded to select the proper RAM.

power-up

After power up, $\overline{RAS}1$ and $\overline{RAS}2$ must remain high for 100 μs immediately prior to initialization. Initialization consists of performing eight $\overline{RAS}$ cycles before proper device operation is achieved.

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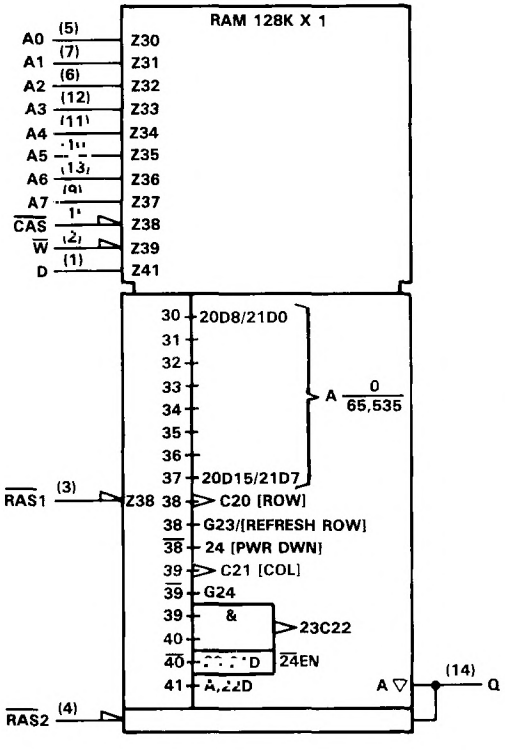
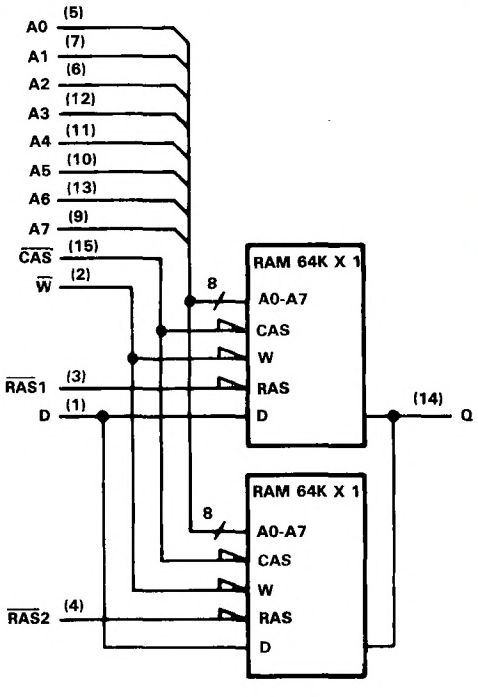
logic symbol†



functional block diagram



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage on any pin except V_{DD} and data out (see Note 1) . . . . . −1.5 V to 10 V
Voltage on V_{DD} supply and data out with respect to V_{SS} . . . . . −1 V to 6 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 2 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values in this data sheet are with respect to V_{SS}.
2. Additional information concerning the handling of ESD sensitive devices is available in a document entitled *"Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies"* in Section 12.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.5	5	5.5	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	V_{DD} = 4.5 V	2.4		4.8	V
		V_{DD} = 5.5 V	2.4		6	
V_{IL}	Low-level input voltage (see Notes 3 and 4)		−0.6		0.8	V
T_A	Operating free-air temperature		0		70	°C

NOTES: 3. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.
4. Due to input protection circuitry, the applied voltage may begin to clamp at −0.6 V. Test conditions must comprehend this occurrence. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All other pins = 0 V			±20	μA
I_O	Output current (leakage)	V_O = 0.4 to 5.5 V, V_{DD} = 5 V, [illegible] high			±20	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		38.5	65	mA
I_{DD2}‡	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		7	10	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ high, All outputs open			90	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, All outputs open			90	mA

† All typical values are at T_A = 25°C and nominal supply voltages.
‡ V_{IL} > −0.6 V.

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capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		TYP†	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs	8	14	pF
$C_{i(D)}$	Input capacitance, data input	8	14	pF
$C_{i(RC)}$	Inpuut capacitance strobe inputs	16	20	pF
$C_{i(W)}$	Input capacitance, write-enable input	16	20	pF
C_o	Output capacitance	10	16	pF

† All typical values are at T_A = 25°C and nominal supply voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	MIN	MAX	UNIT
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		85	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, Load = 2 Series 74 TTL gates	t_{RAC}		150	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	40	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	MIN	MAX	UNIT
$t_{c(P)}$	Page-mode cycle time	t_{PC}			ns
$t_{c(rd)}$	Read cycle time†	t_{RC}			ns
$t_{c(W)}$	Write cycle time	t_{WC}			ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	315		ns
$t_{w(CH)}$	Pulse duration, CAS high (precharge time)‡	t_{CP}	60		ns
$t_{w(CL)}$	Pulse duration, CAS low§	t_{CAS}	85	10,000	ns
$t_{w(RH)}$	Pulse duration, RAS high (precharge time)	t_{RP}			ns
$t_{w(RL)}$	Pulse duration, RAS low¶	t_{RAS}		10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}			ns
t_t	Transition times (rise and fall) for RAS and CAS	t_T	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		ns
$t_{su(WCH)}$	Write-command setup time before CAS high	t_{CWL}	55		ns
$t_{su(WRH)}$	Write-command setup time before RAS high	t_{RWL}	55		ns
$t_{h(CLCA)}$	Column-address hold time after CAS low	t_{CAH}	45		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	20		ns
$t_{h(RLCA)}$	Column-address hold time after RAS low	t_{AR}	110		ns
$t_{h(CLD)}$	Data hold time after CAS low	t_{DH}	45		ns
$t_{h(RLD)}$	Data hold time after RAS low	t_{DHR}	120		ns
$t_{h(WLD)}$	Data hold time after W low	t_{DH}	45		ns
$t_{h(CHrd)}$	Read-command hold time after CAS high	t_{RCH}	0		ns
$t_{h(RHrd)}$	Read-command hold time after RAS high	t_{RRH}	20		ns
$t_{h(CLW)}$	Write-command hold time after CAS low	t_{WCH}	60		ns
$t_{h(RLW)}$	Write-command hold time after RAS low	t_{WCR}	120		ns
t_{RLCH}	Delay time, RAS low to CAS high	t_{CSH}	150		ns
t_{CHRL}	Delay time, CAS high to RAS low	t_{CRP}	10		ns
t_{CLRH}	Delay time, RAS low to CAS high	t_{RSH}	85		ns
t_{CLWL}	Delay time, CAS low to W low (read-modify-write cycle only)	t_{CWD}	75		ns
t_{RLCL}	Delay time, RAS low to CAS low (maximum value specified only to guarantee access time)	t_{RCD}	30	65	ns
t_{RLWL}	Delay time, RAS low to W low (read-modify-write cycle only)	t_{RWD}	150		ns
t_{WLCL}	Delay time, W low to CAS low (early write cycle)	t_{WCS}	0		ns
t_{rf}	Refresh time interval	t_{REF}		4	ms

NOTE 5: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

† All cycle times assume t_t = 5 ns.

‡ Page mode only.

§ In read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional CAS low time ($t_{w(CL)}$). This applies to page-mode read-modify-write cycles also.

¶ In read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional RAS low time ($t_{w(RL)}$).

PARAMETER MEASUREMENT INFORMATION

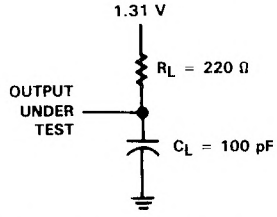
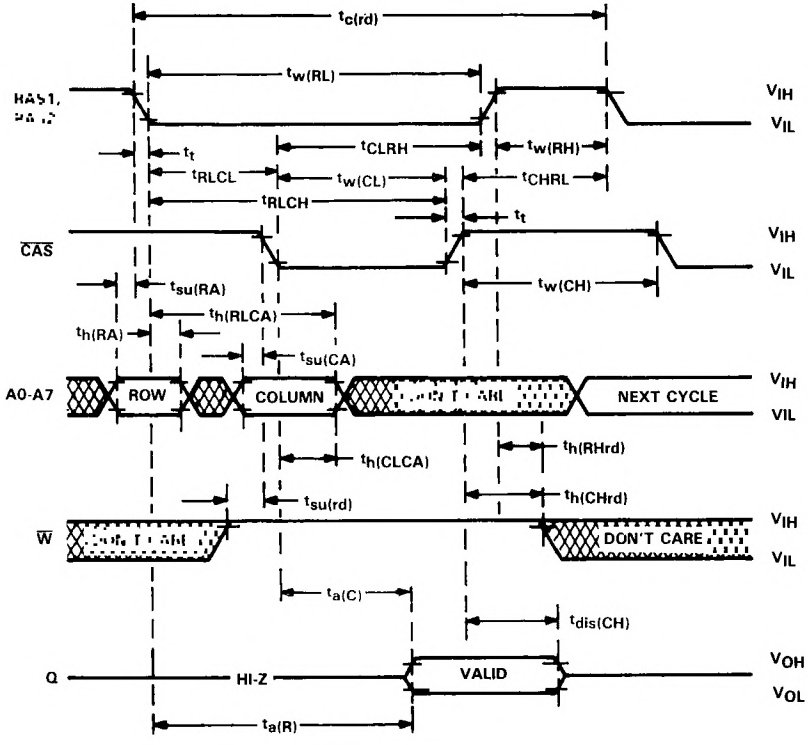
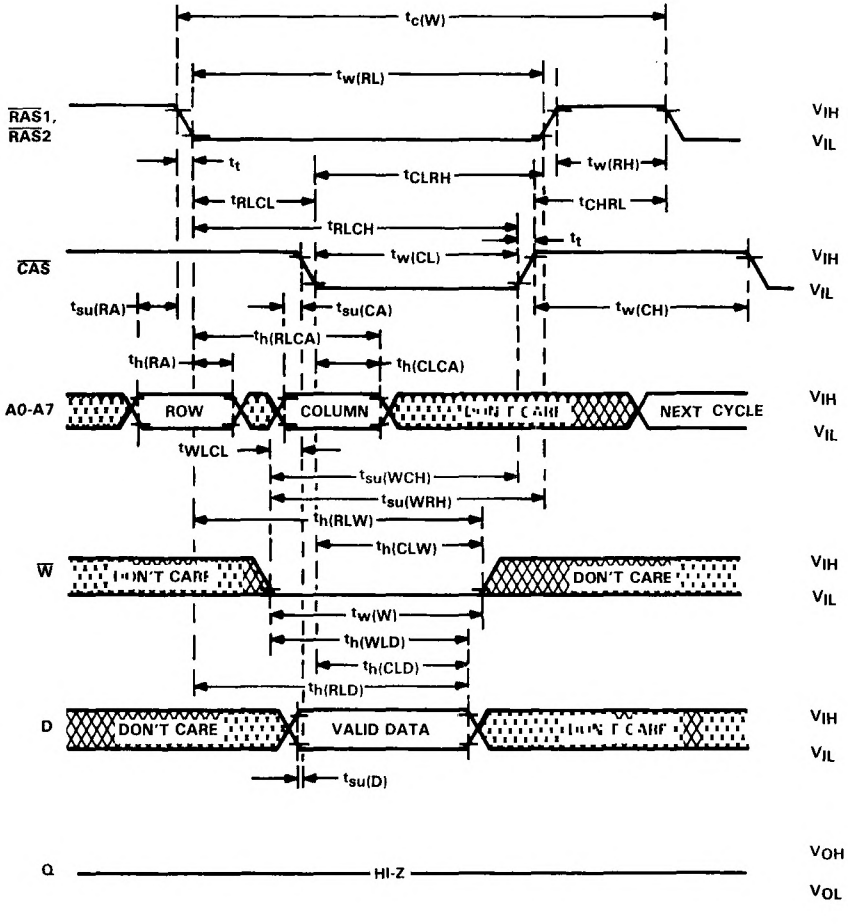


FIGURE 1. LOAD CIRCUIT

read cycle timing



early write cycle timing



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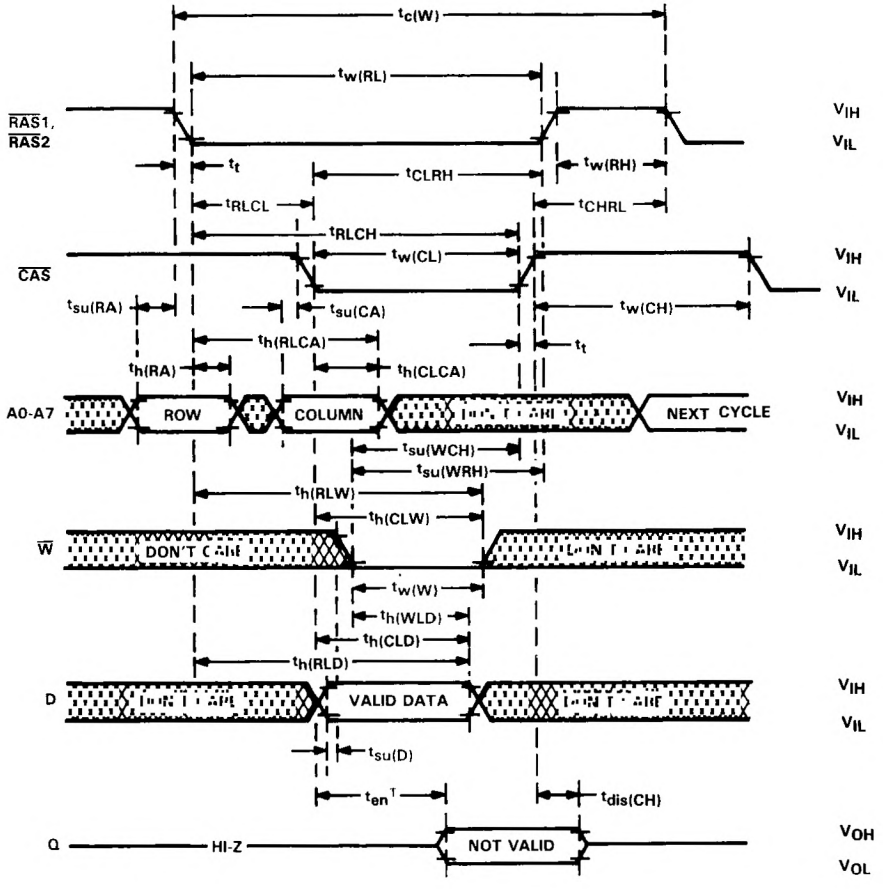
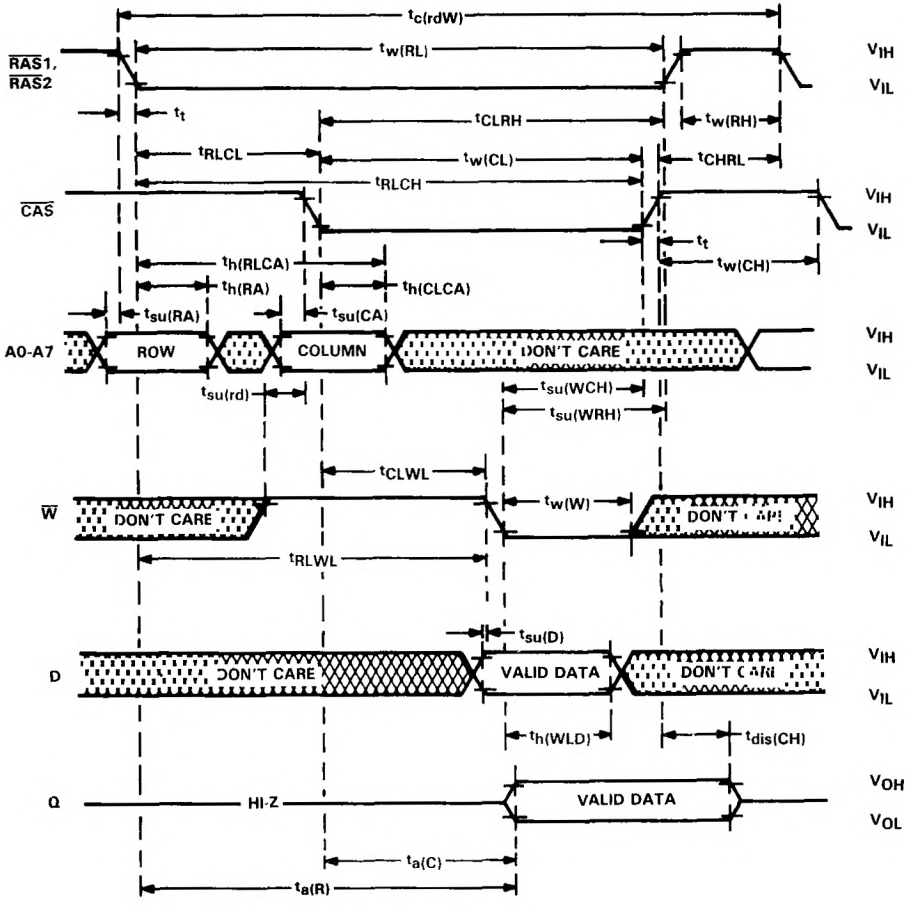
write cycle timing



† The enable time (t_{en}) for a write cycle is equal in duration to the access time from $\overline{CAS}$ ($t_{a(C)}$) in a read cycle; but the active levels at the output are invalid.

read-modify-write cycle timing



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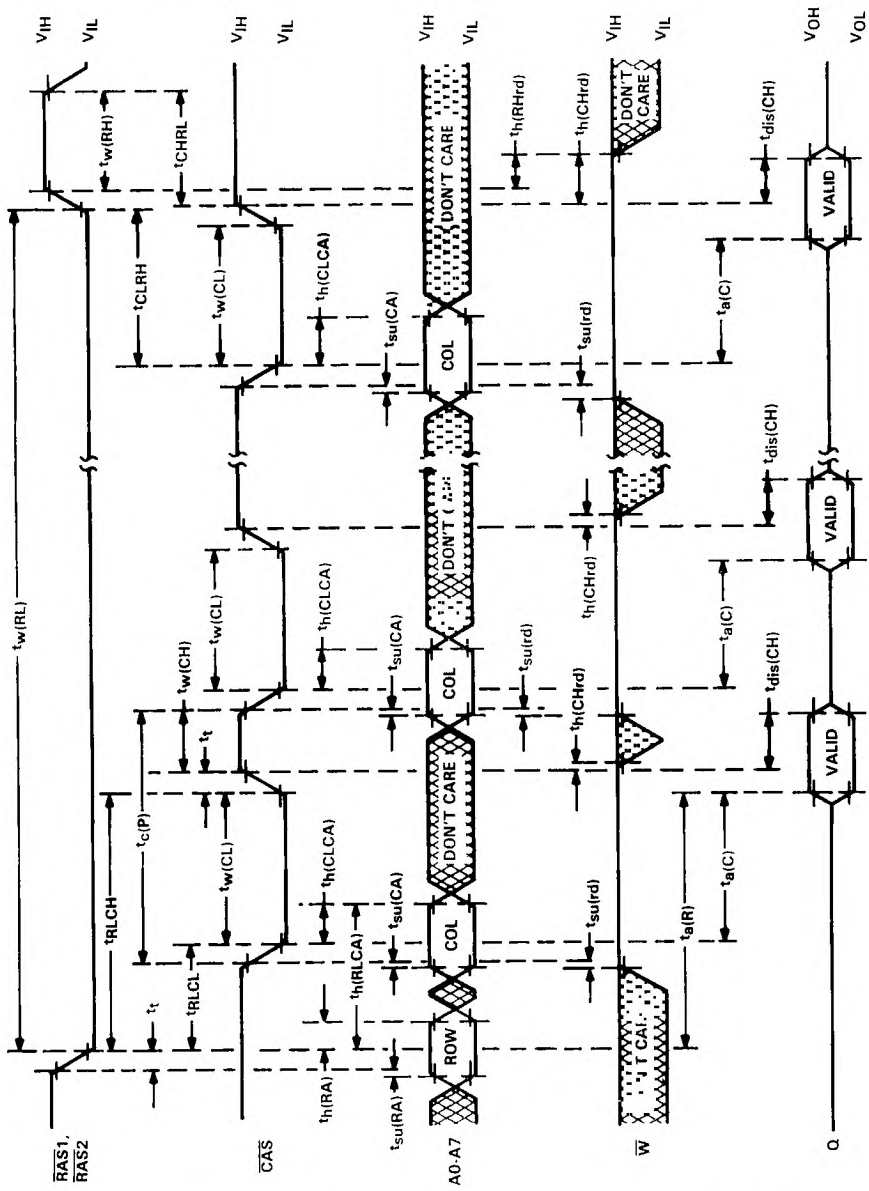
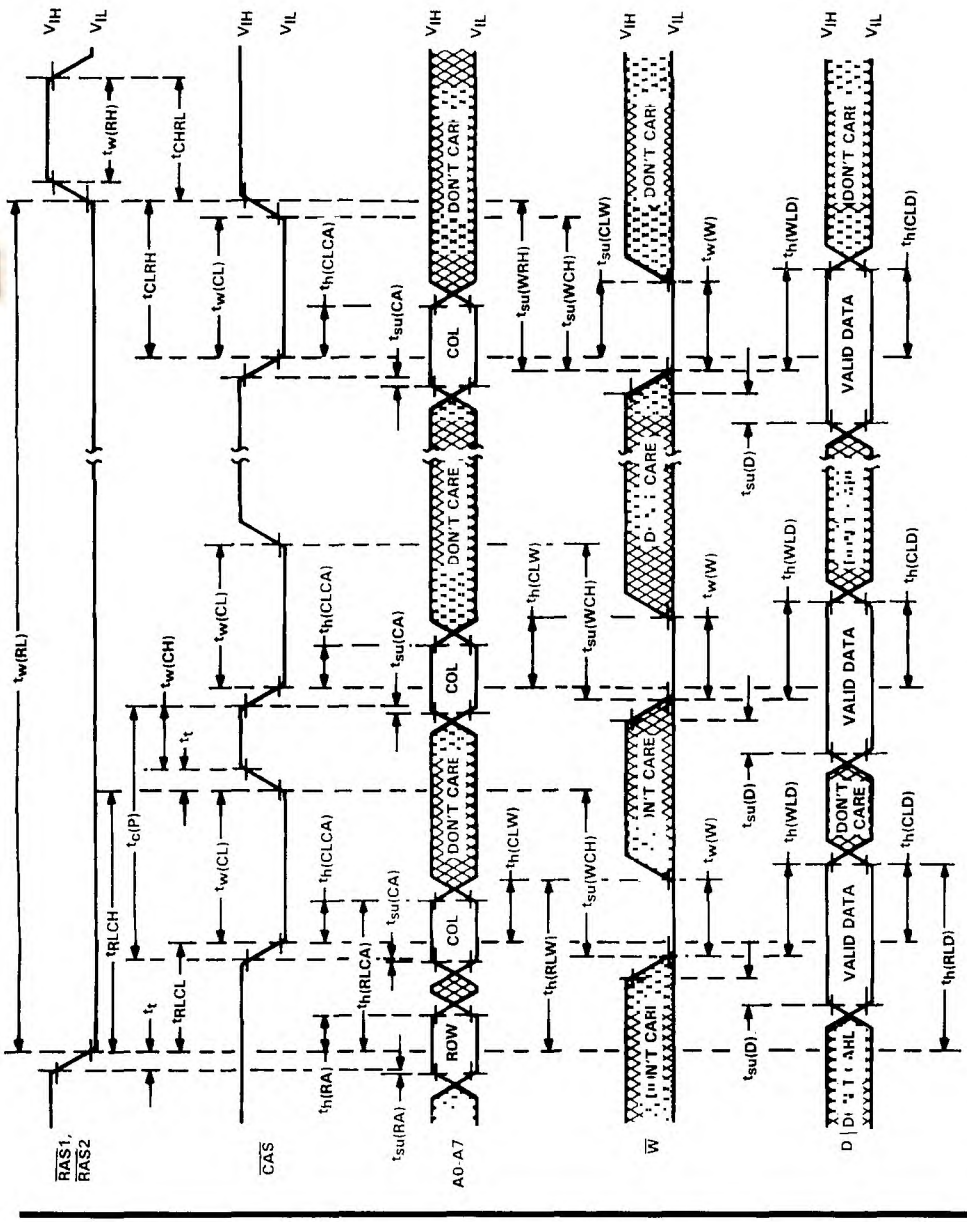
page-mode read cycle timing



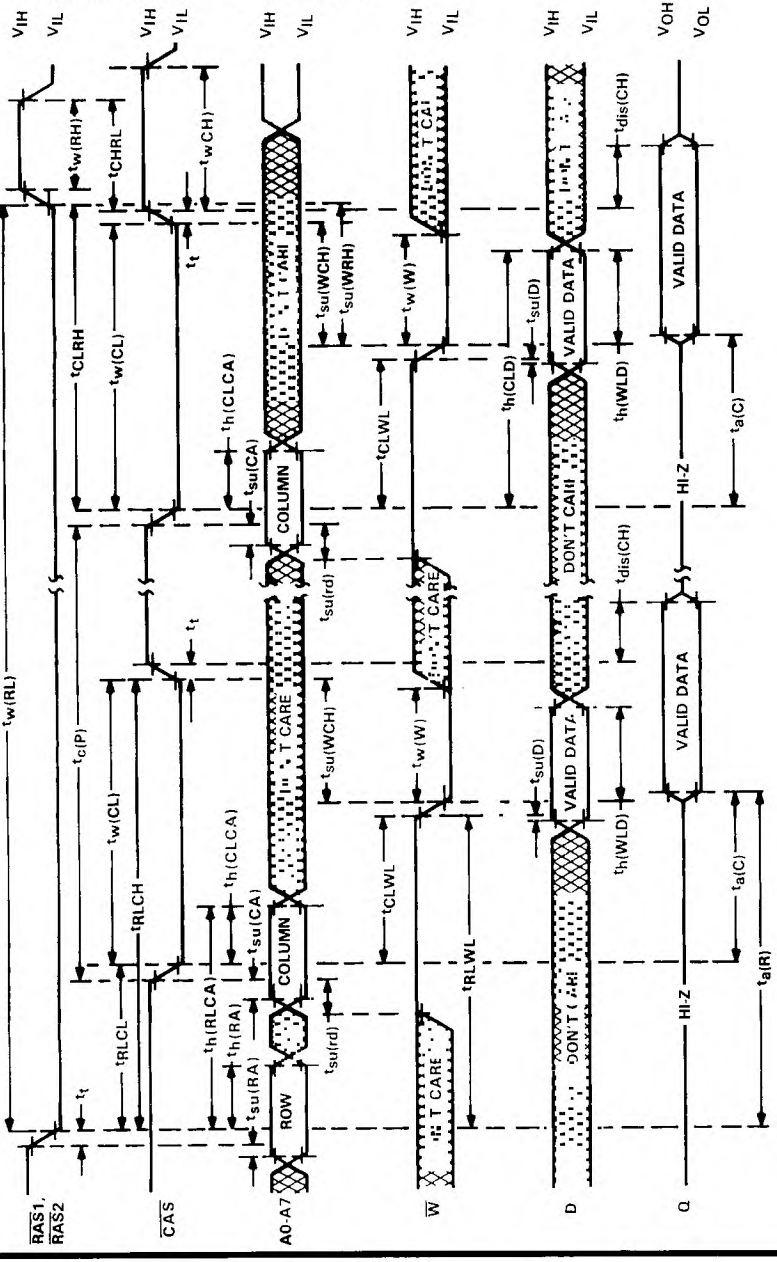
NOTE 6: A write cycle or a read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

page-mode write cycle timing



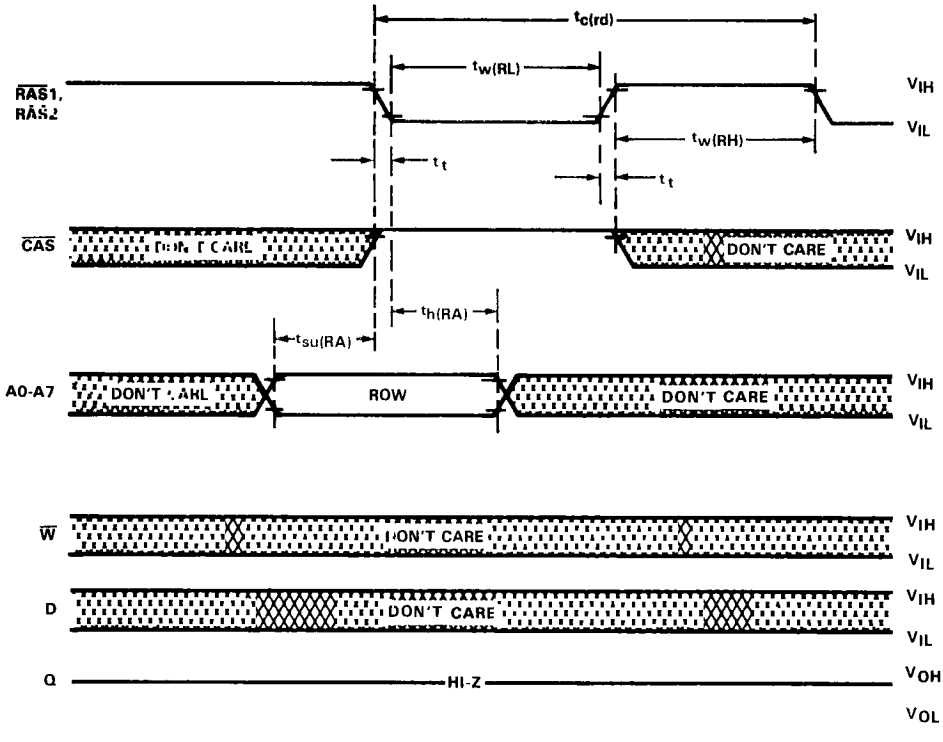
NOTE 7: A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as the read and read-modify-write timing specifications are not violated.

page-mode read-modify-write cycle timing



NOTE 8: A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

$\overline{\text{RAS}}$-only refresh timing



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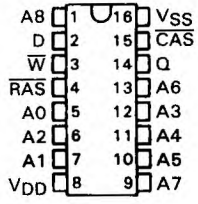
MAY 1983—REVISED NOVEMBER 1985

- 262,144 X 1 Organization
- Single 5-V Supply (10% Tolerance)
- JEDEC Standardized Pinout
- Upward Pin Compatible with TMS4164 (64K Dynamic RAM)
- Performance Ranges:

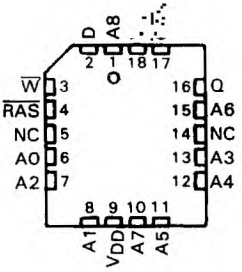
DEVICE	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)
TMS4256-12 TMS4257-12	120 ns	60 ns	230 ns
TMS4256-15 TMS4257-15	150 ns	75 ns	260 ns
TMS4256-20 TMS4257-20	200 ns	100 ns	330 ns

- Long Refresh Period . . . 4 ms (Max)
- Low Refresh Overhead Time . . . As Low As 1.3% of Total Refresh Period
- On-Chip Substrate Bias Generator
- Operations of the TMS4256/TMS4257 Can Be Controlled by TI's THCT4502 Dynamic RAM Controller
- All Inputs, Outputs, and Clocks Fully TTL Compatible
- 3-State Unlatched Output
- Common I/O Capability with "Early Write" Feature
- Page ('4256) or Nibble-Mode ('4257) Options for Faster Access Operation
- Power Dissipation As Low As
  —Operating . . . 275 mW (Typ)
  —Standby . . . 12.5 mW (Typ)
- $\overline{RAS}$-Only Refresh Mode
- Hidden Refresh Mode

N PACKAGE
(TOP VIEW)



FM PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
NC	No Connection
Q	Data Out
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

- $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Mode
- Available with MIL-STD-883B Processing and L(0°C to 70°C), E(−40°C to 85°C), or S(−55°C to 100°C) Temperature Ranges

description

The '4256 and '4257 are high-speed, 262,144-bit dynamic random-access memories, organized as 262,144 words of one bit each. They employ state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon/polycide gate technology for very high performance combined with low cost and improved reliability.

These devices feature maximum $\overline{RAS}$ access times of 120 ns, 150 ns, or 200 ns. Typical power dissipation is as low as 275 mW operating and 12.5 mW standby.

New SMOS technology permits operation from a single 5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{DD} peaks are 125 mA typical, and a −1-V input voltage undershoot can be tolerated, minimizing system noise considerations.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address and data-in lines are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The '4256 and '4257 are offered in 16-pin plastic dual-in-line and 18-lead plastic chip carrier packages. They are guaranteed for operation from 0°C to 70°C. The dual-in-line package is designed for insertion in mounting-hole rows on 7,62-mm (300-mil) centers.

operation

address (A0 through A8)

Eighteen address bits are required to decode 1 of 262,144 storage cell locations. Nine row-address bits are set up on pins A0 through A8 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the nine column-address bits are set up on pins A0 through A8 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (D)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data out (Q)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In a read-modify-write cycle, the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least once every four milliseconds to retain data. This can be achieved by strobing each of the 256 rows (A0-A7). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state.

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$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh

The $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh is utilized by bringing $\overline{\text{CAS}}$ low earlier than $\overline{\text{RAS}}$ (see parameter t_{CLRL}) and holding it low after $\overline{\text{RAS}}$ falls (see parameter t_{RLCHR}). For successive $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycles, $\overline{\text{CAS}}$ can remain low while cycling $\overline{\text{RAS}}$. The external address is ignored and the refresh address is generated internally.

hidden refresh

Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{\text{CAS}}$ at V_{IL} after a read operation and cycling $\overline{\text{RAS}}$ after a specified precharge period, similar to a "$\overline{\text{RAS}}$-only" refresh cycle. The external address is also ignored during the hidden refresh cycles.

page mode (TMS4256)

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing random column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. The maximum number of columns that can be addressed is determined by $t_{w(RL)}$, the maximum $\overline{\text{RAS}}$ low pulse duration.

nibble mode (TMS4257)

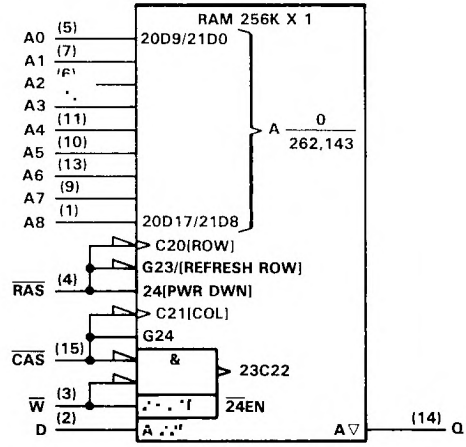
Nibble-mode operation allows high-speed serial read, write, or read-modify-write access of 1 to 4 bits of data. The first bit is accessed in the normal manner with read data coming out at $t_{a(C)}$ time. The next sequential nibble bits can be read or written by cycling $\overline{\text{CAS}}$ while $\overline{\text{RAS}}$ remains low. The first bit is determined by the row and column addresses, which need to be supplied only for the first access. Column A8 and row A8 (CA8, RA8) provide the two binary bits for initial selection of the nibble addresses. Thereafter, the falling edge of $\overline{\text{CAS}}$ will access the next bit of the circular 4-bit nibble in the following sequence:

In nibble-mode, all normal memory operations (read, write, or ready-modify-write) may be performed in any desired combination.

power-up

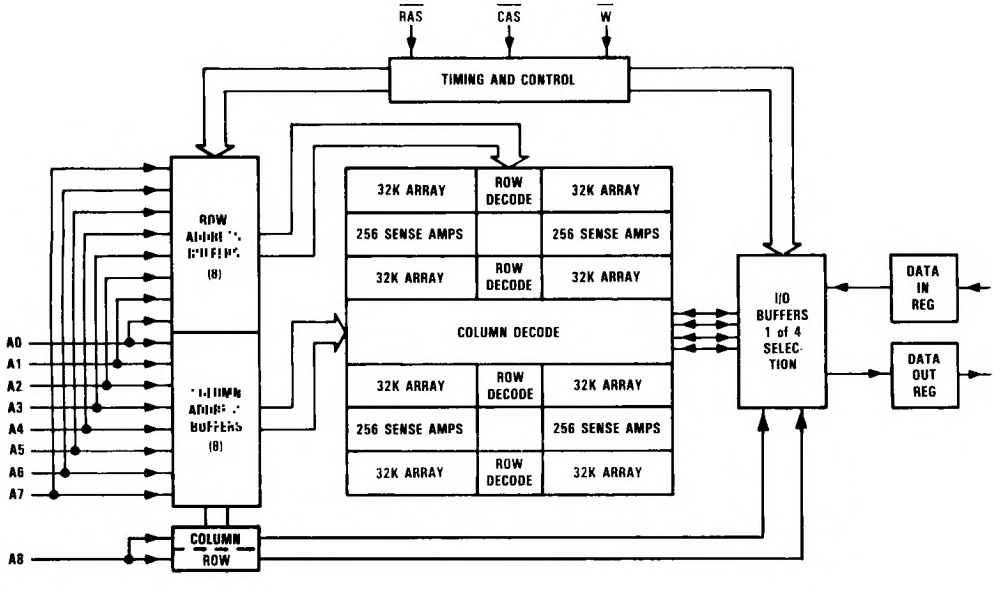
To achieve proper device operation, an initial pause of 200 μs is required after power up followed by a minimum of eight initialization cycles.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown are for the 16-pin dual-in-line package.

functional block diagram



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range for any pin including V_{DD} supply (see Note 1) . . . . . −1 V to 7 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as maximum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS4256-12 TMS4257-12 MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{DD} = 5 V, All other pins = 0 V to 6.5 V			±10	μA
I_O	Output current (leakage)	V_O = 0 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, Output open		65	78	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, Output open		2.5	4.5	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high, Output open		45	60	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, Output open		35	48	mA
I_{DD5}	Average nibble-mode current	$t_{c(N)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, Output open		32	44	mA

PARAMETER		TEST CONDITIONS	TMS4256-15 TMS4257-15 MIN	TYP†	MAX	TMS4256-20 TMS4257-20 MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{DD} = 5 V, All other pins = 0 V to 6.5 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, Output open		55	68		45	58	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, Output open		2.5	4.5		2.5	4.5	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high, Output open		40	53		35	48	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, Output open		30	43		25	35	mA
I_{DD5}	Average nibble-mode current	$t_{c(N)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, Output open		27	39		22	32	mA

†All typical values are at T_A = 25°C and nominal supply voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		TYP†	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs	4	7	pF
$C_{i(D)}$	Input capacitance, data input	4	7	pF
$C_{i(RC)}$	Input capacitance strobe inputs	4	8	pF
$C_{i(W)}$	Input capacitance, write enable input	4	8	pF
C_o	Output capacitance	5	10	pF

†All typical values are at T_A = 25°C and nominal supply voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS4256-12 TMS4257-12		UNIT
				MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{RLCL} \geq$ MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		60	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{RAC}		120	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	30	ns

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS4256-15 TMS4257-15		TMS4256-20 TMS4257-20		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{RLCL} \geq$ MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		75		100	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{RAC}		150		200	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	30	0	35	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TMS4256-12 TMS4257-12		UNIT
			MIN	MAX	
$t_{c(P)}$	Page-mode cycle time (read or write cycle)	t_{PC}	[illegible]		ns
$t_{c(PM)}$	Page-mode cycle time (read-modify-write cycle)	t_{PCM}	[illegible]		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	230		ns
$t_{c(W)}$	Write cycle time	t_{WC}	230		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	275		ns
$t_{w(CH)P}$	Pulse duration, [illegible] high (page mode)	t_{CP}	50		ns
$t_{w(CH)}$	Pulse duration, [illegible] high (non-page mode)	t_{CPN}	25		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low‡	t_{CAS}	60	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	100		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low§	t_{RAS}	120	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	40		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		ns
$t_{su(WCL)}$	Early write-command setup time before $\overline{CAS}$ low	t_{WCS}	0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	40		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	40		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	20		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	80		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	35		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	95		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	35		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	35		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	95		ns

Continued next page.

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.

†All cycle times assume t_t = 5 ns.

‡In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page-mode read-modify-write also.

§In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

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timing requirements over recommended supply voltage range and operating free-air temperature range (continued)

		ALT. SYMBOL	TMS4256-12 TMS4257-12		UNIT
			MIN	MAX	
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	120		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	60		ns
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high¶	t_{CHR}	25		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low¶	t_{CSR}	25		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low¶	t_{RPC}	20		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	60		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	60	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	120		ns
t_{rf}	Refresh time interval	t_{REF}		4	ms

Continued next page.

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.

¶$\overline{CAS}$-before-$\overline{RAS}$ refresh only.

timing requirements over recommended supply voltage range and operating free-air temperature range (continued)

		ALT. SYMBOL	TMS4256-15 TMS4257-15		TMS4256-20 TMS4257-20		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time (read or write cycle)	t_{PC}	145		190		ns
$t_{c(PM)}$	Page-mode cycle time (read-modify-write cycle)	t_{PCM}	190		245		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	260		330		ns
$t_{c(W)}$	Write cycle time	t_{WC}	260		330		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	305		370		ns
$t_{w(CH)P}$	Pulse duration, $\overline{CAS}$ high (page mode)	t_{CP}	60		80		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (non-page mode)	t_{CPN}	25		30		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low‡	t_{CAS}	75	10,000	100	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	100		120		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low§	t_{RAS}	150	10,000	200	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	45		55		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCL)}$	Early write-command setup time before $\overline{CAS}$ low	t_{WCS}	0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	45		60		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	45		60		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	25		30		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		20		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	100		130		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	45		55		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	120		155		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	45		55		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		15		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	45		55		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	120		155		ns

Continued next page.

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.

†All cycle times assume t_t = 5 ns.

‡In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page-mode read-modify-write also.

§In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

timing requirements over recommended supply voltage range and operating free-air temperature range (concluded)

		ALT. SYMBOL	TMS4256-15 TMS4257-15		TMS4256-20 TMS4257-20		UNIT
			MIN	MAX	MIN	MAX	
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	75		100		ns
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high¶	t_{CHR}	30		35		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low¶	t_{CSR}	30		35		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low¶	t_{RPC}	20		25		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	70		90		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	75	30	100	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	145		190		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

NOTE 3: Timing measurements are referenced to V_{IL} max and V_{IH} min.
¶$\overline{CAS}$-before-$\overline{RAS}$ refresh only.

NIBBLE-MODE CYCLE

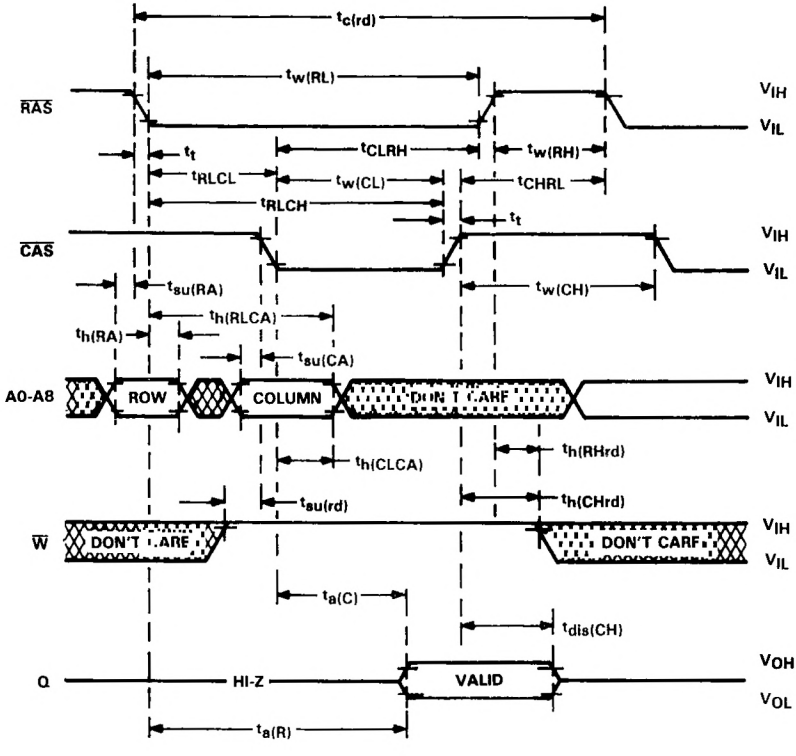
switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		ALT. SYMBOL	TMS4257-12		TMS4257-15		TMS4257-20		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(CN)}$	Nibble-mode access time from $\overline{CAS}$	t_{NCAC}		30		40		50	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TMS4257-12		TMS4257-15		TMS4257-20		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(N)}$	Nibble-mode cycle time	t_{NC}	60		75		90		ns
$t_{c(rdWN)}$	Nibble-mode read-modify-write cycle time	t_{NRMW}	85		105		130		
t_{CLRHN}	Nibble-mode delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{NRSH}	30		40		50		
t_{CLWLN}	Nibble-mode delay time, $\overline{CAS}$ to $\overline{W}$ delay	t_{NCWD}	25		30		40		
$t_{w(CLN)}$	Nibble-mode pulse duration, $\overline{CAS}$ low	t_{NCAS}	30		40		50		
$t_{w(CHN)}$	Nibble-mode pulse duration, $\overline{CAS}$ high	t_{NCP}	20		25		30		
$t_{w(CRWN)}$	Nibble-mode read-modify-write pulse duration, $\overline{CAS}$ low	t_{NCRW}	55		70		90		
$t_{su(WCHN)}$	Nibble-mode write command setup time before $\overline{CAS}$ high	t_{NCWL}	25		35		45		

read cycle timing



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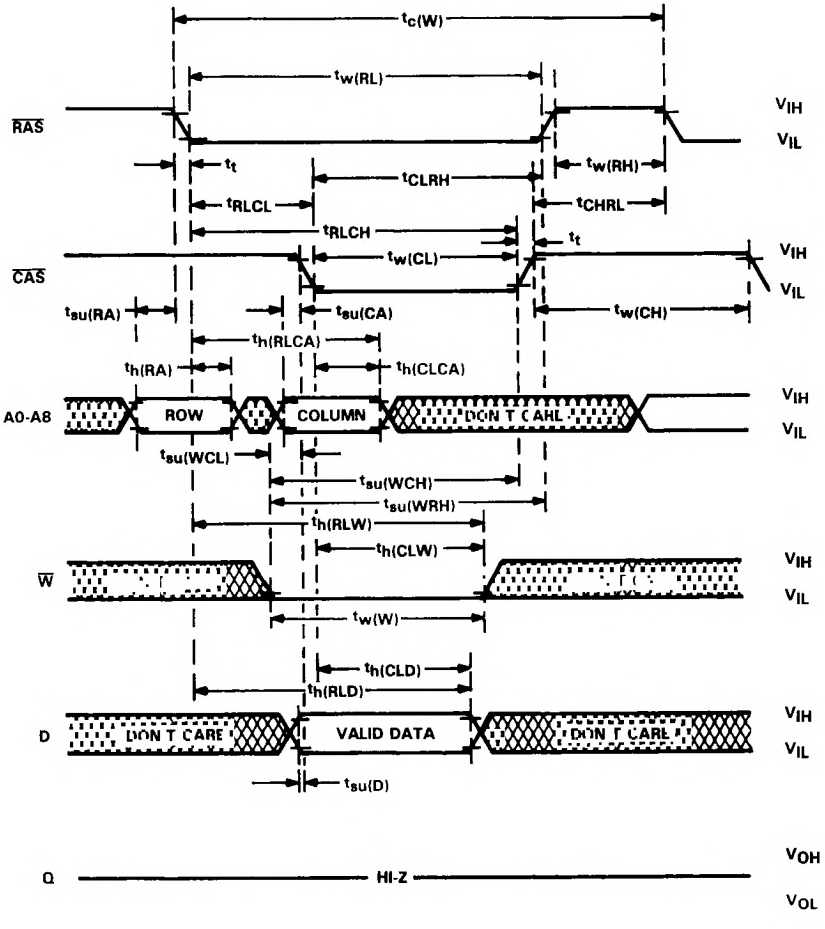
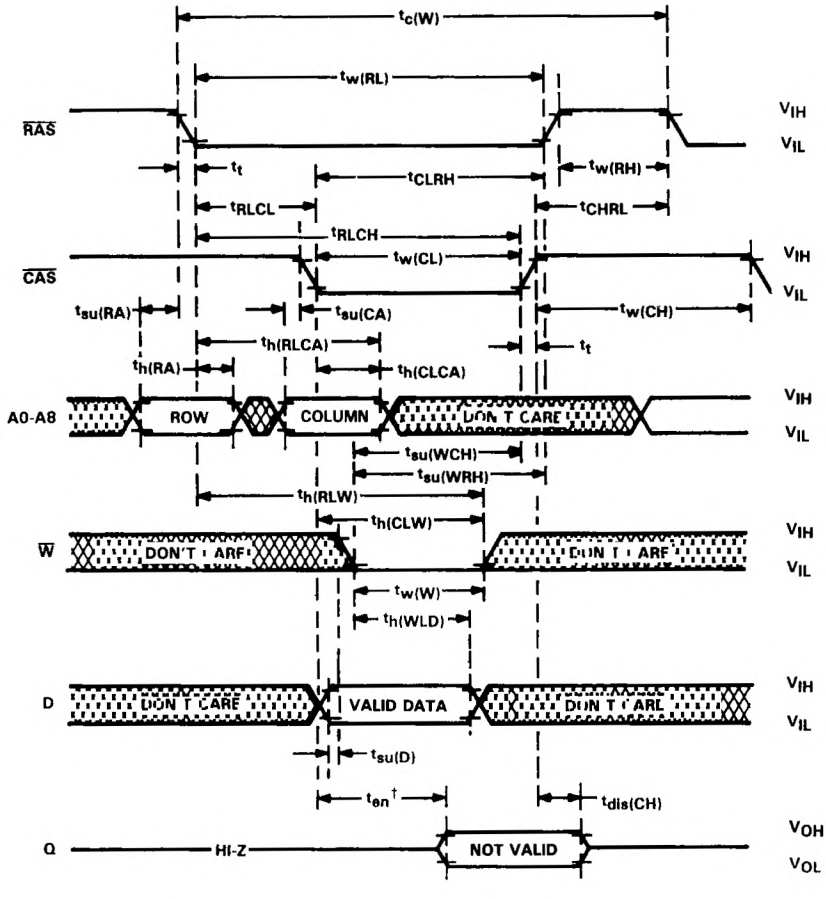
early write cycle timing



write cycle timing



†The enable time (t_{en}) for a write cycle is equal in duration to the access time from $\overline{CAS}$ ($t_{a(C)}$) in a read cycle; but the active levels at the output are invalid.

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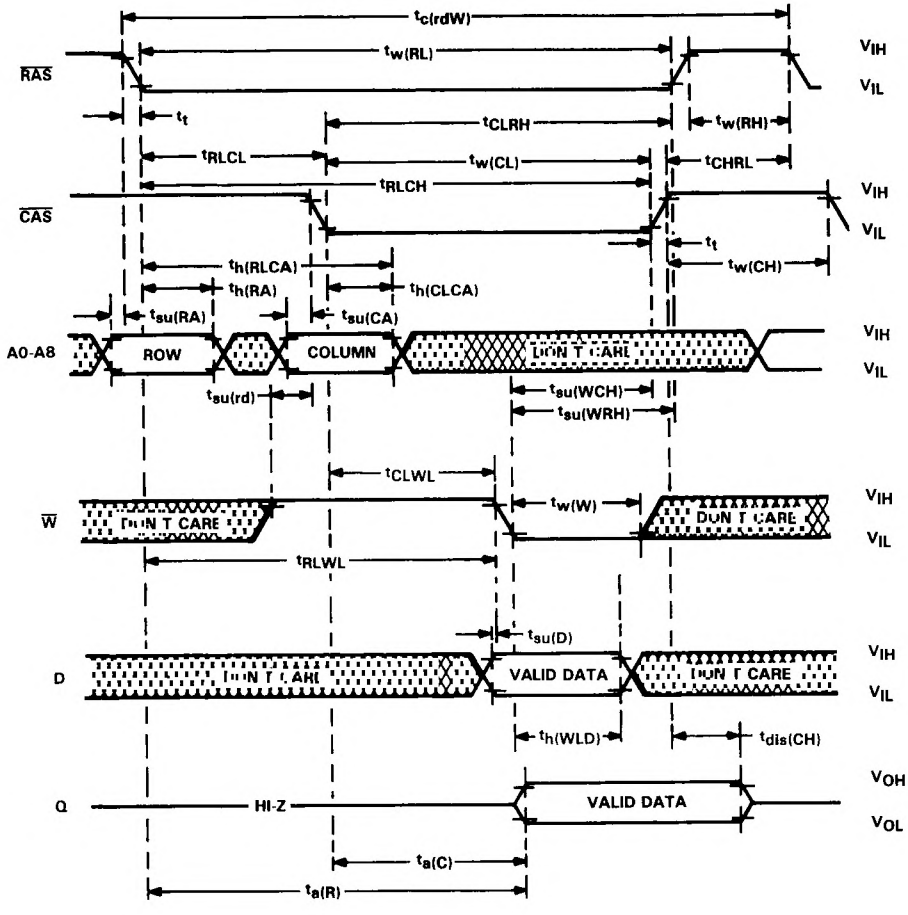
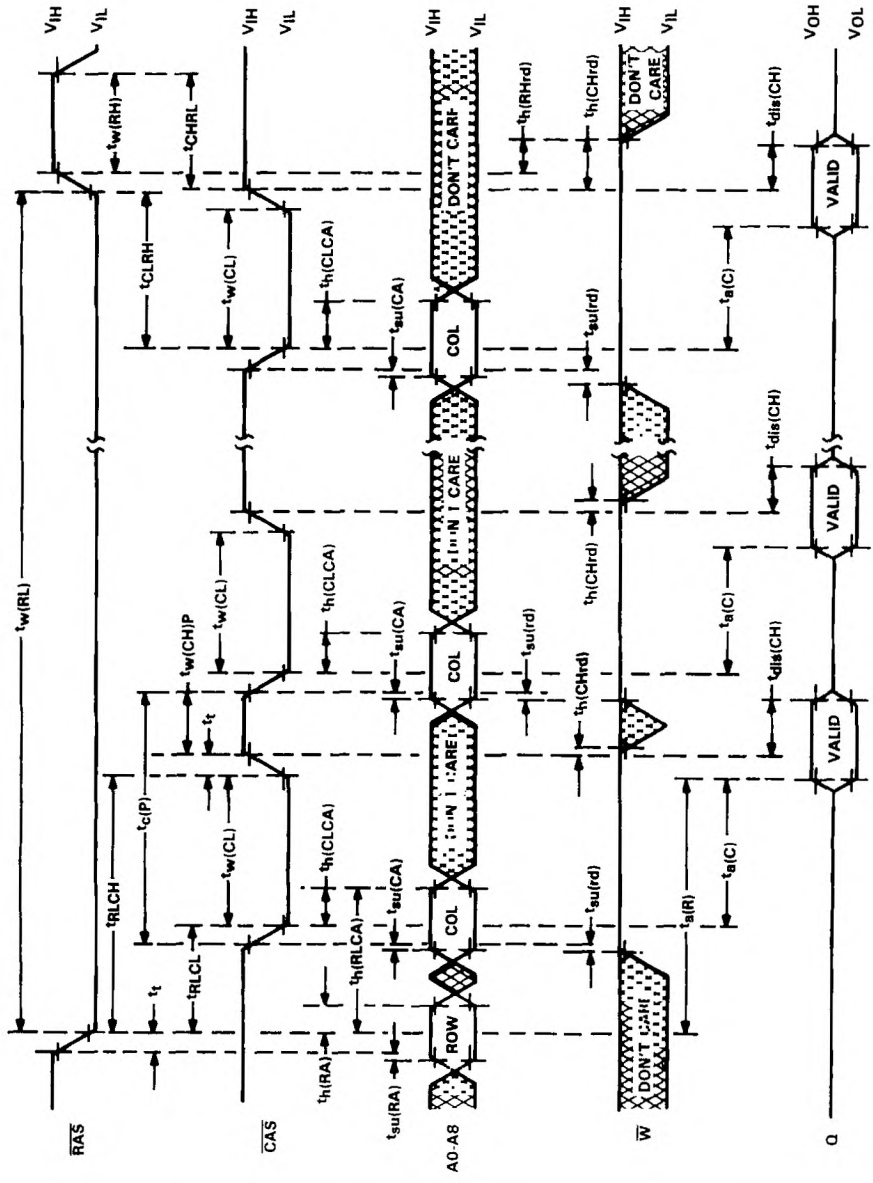
read-write/read-modify-write cycle timing

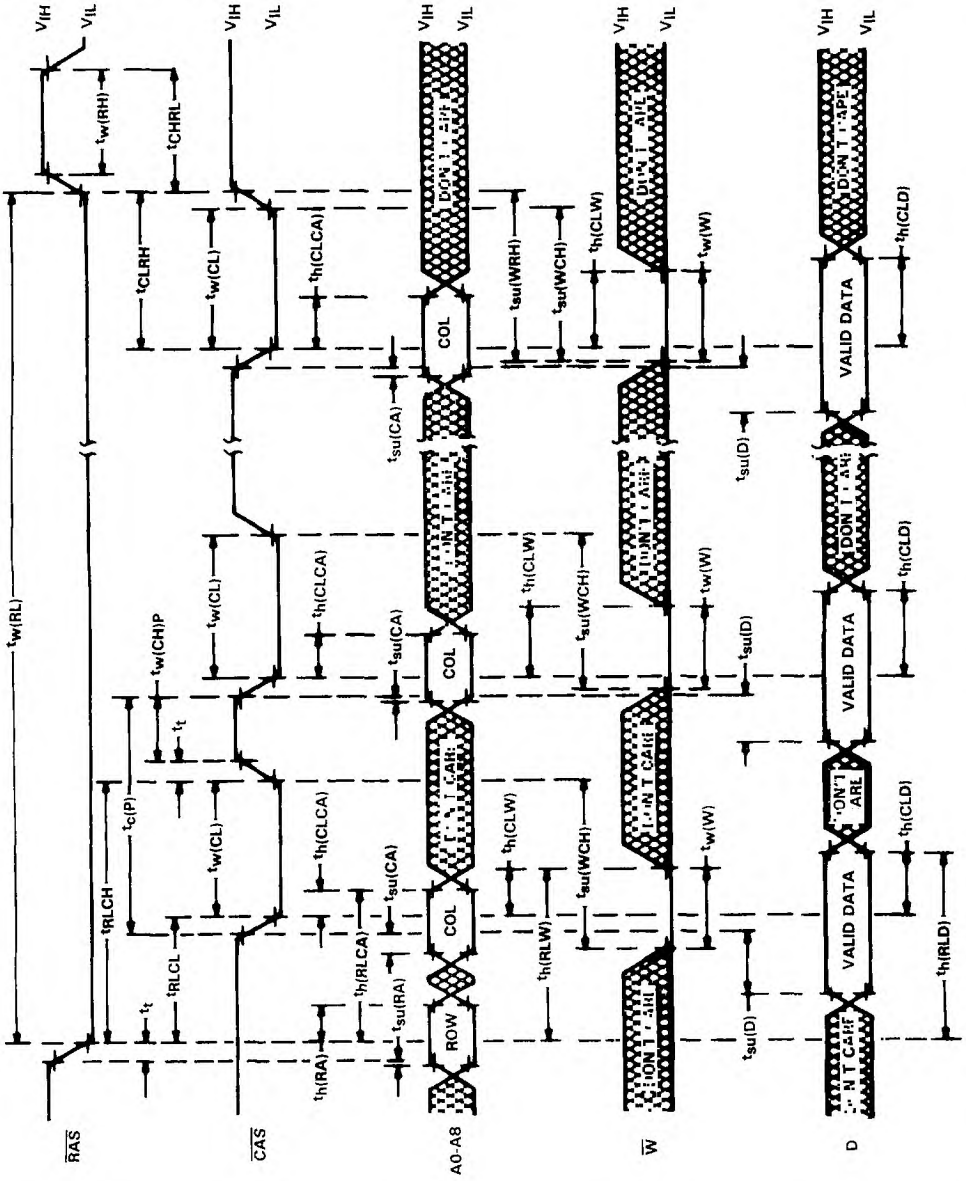


page-mode read cycle timing



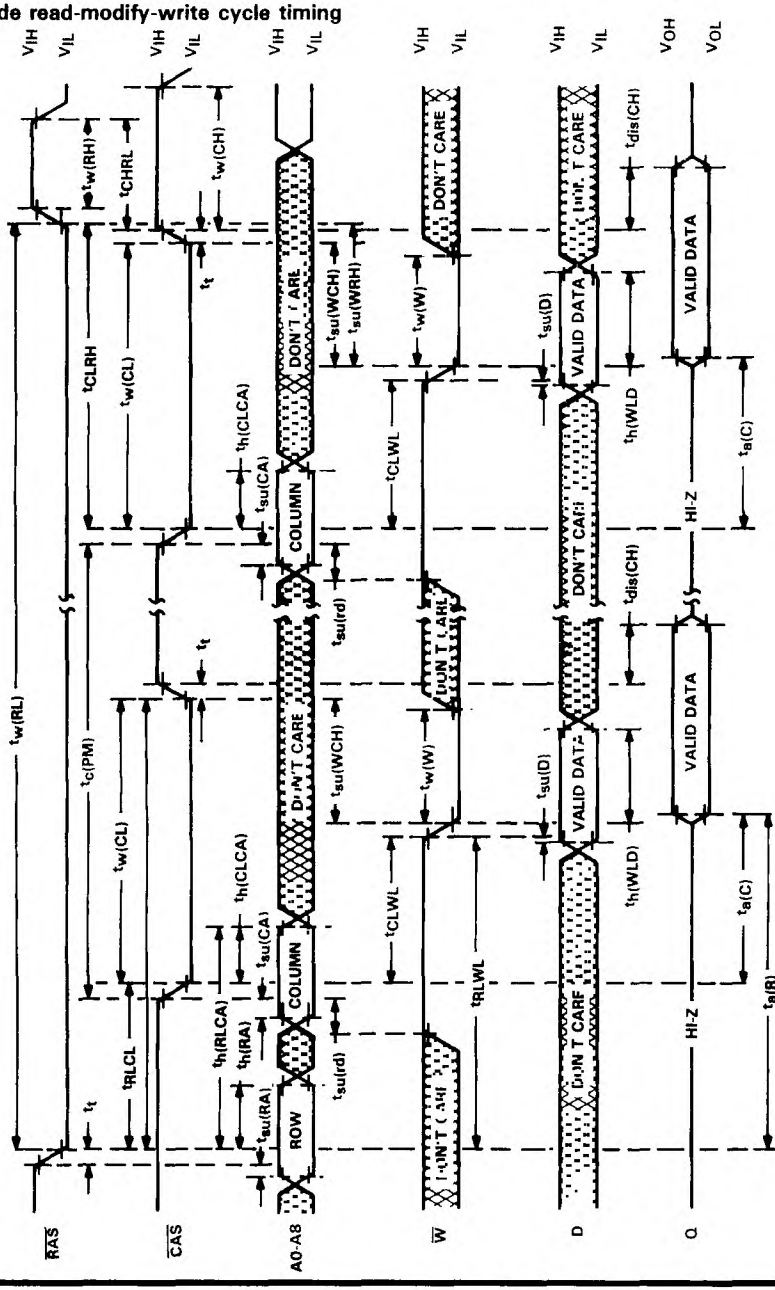
NOTE 4: A write cycle or a read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

page-mode write cycle timing



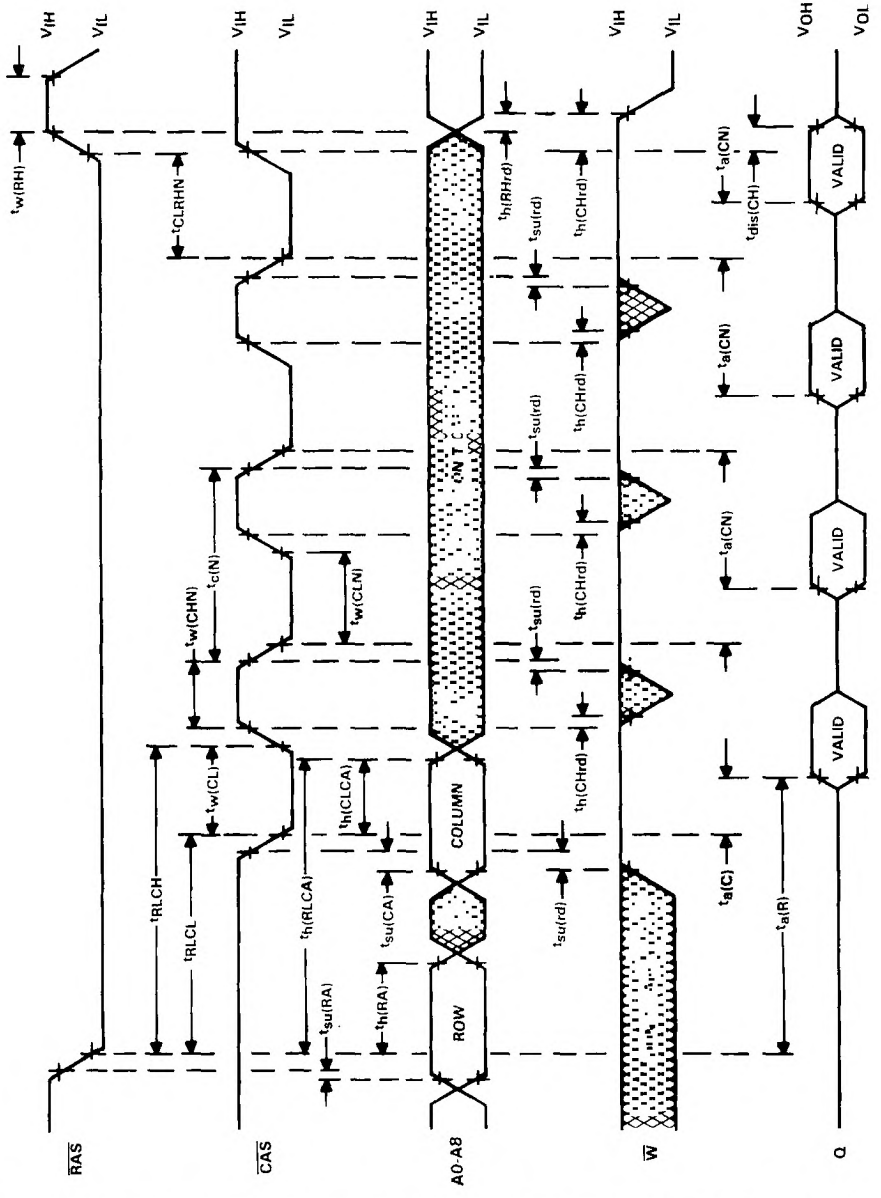
NOTE 5: A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as read and read-modify-write timing specifications are not violated.

page-mode read-modify-write cycle timing

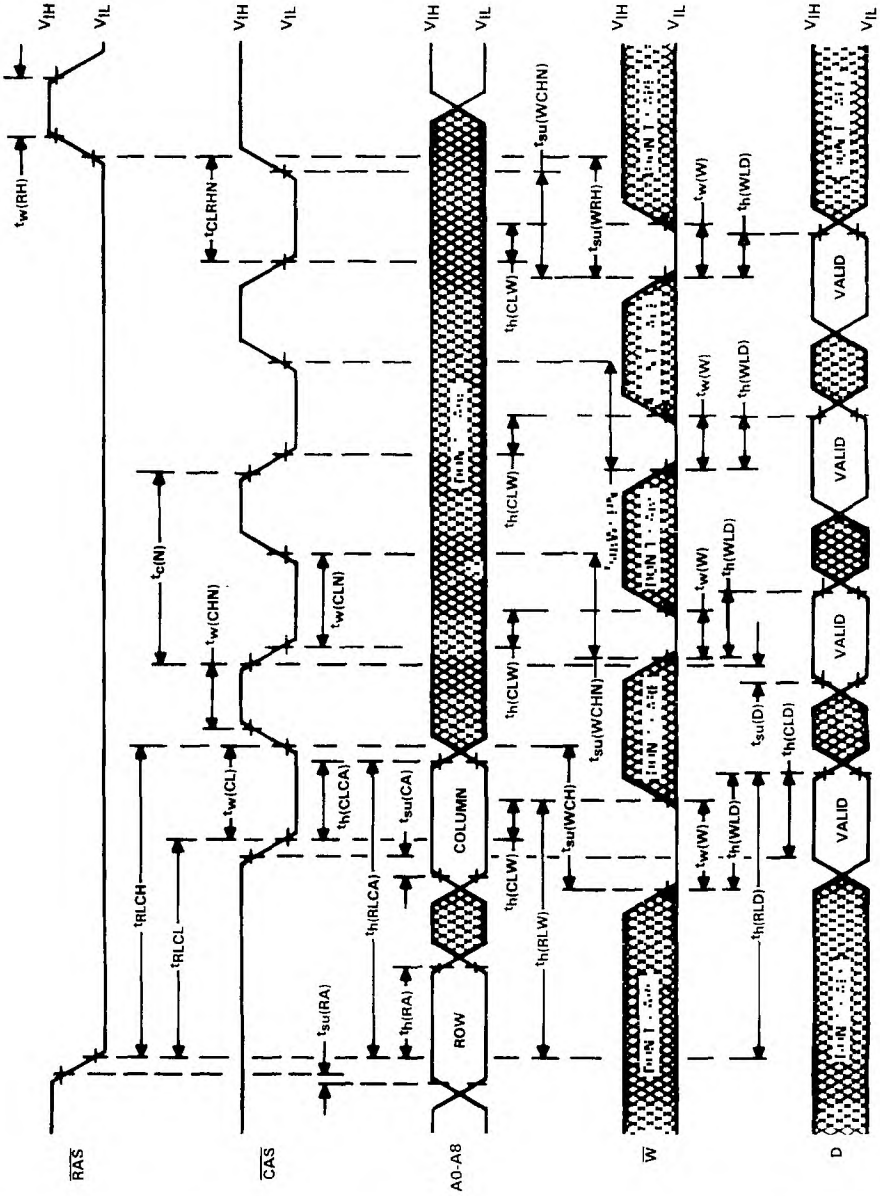


NOTE 6: A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

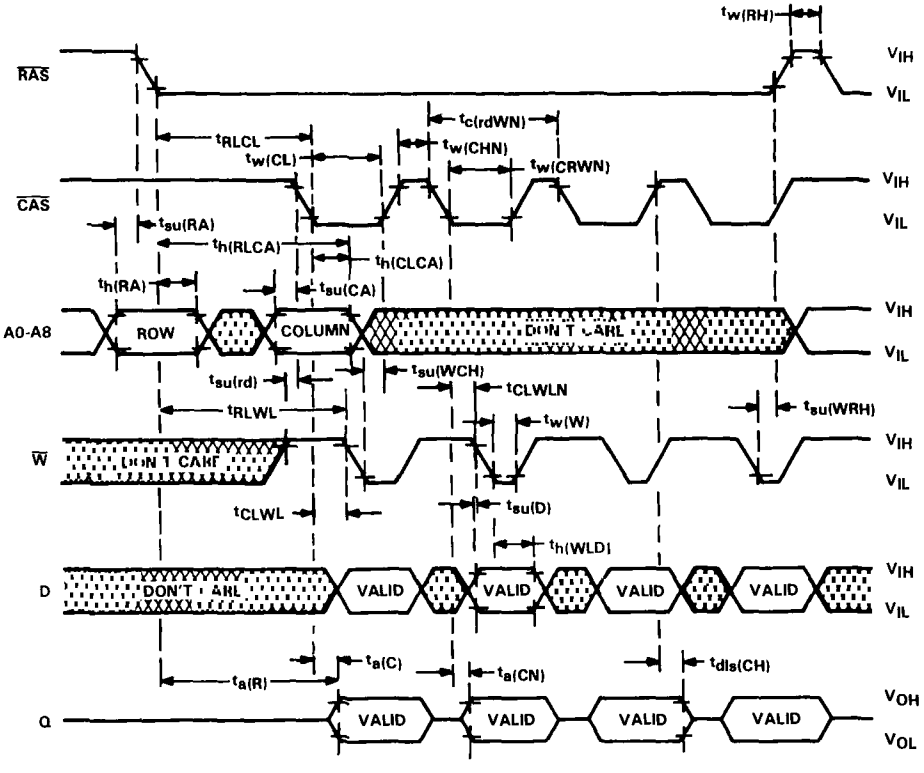
nibble-mode read cycle timing



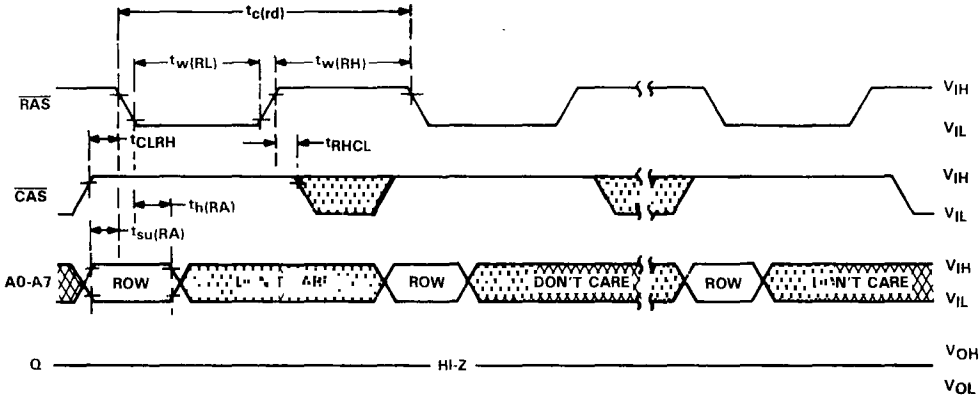
nibble-mode write cycle timing



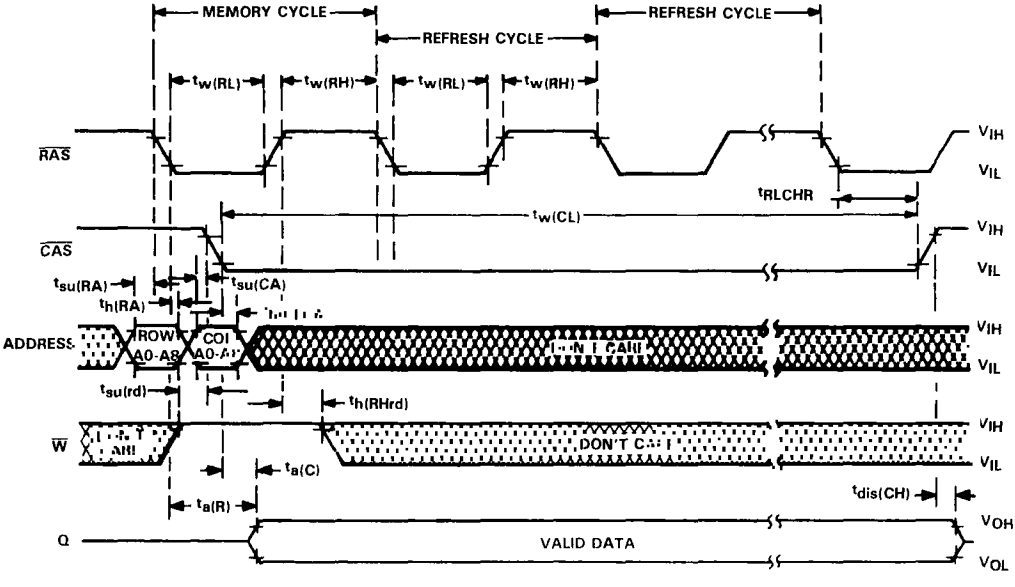
nibble-mode read-modify-write-cycle timing



RAS-only refresh cycle timing



hidden refresh cycle timing



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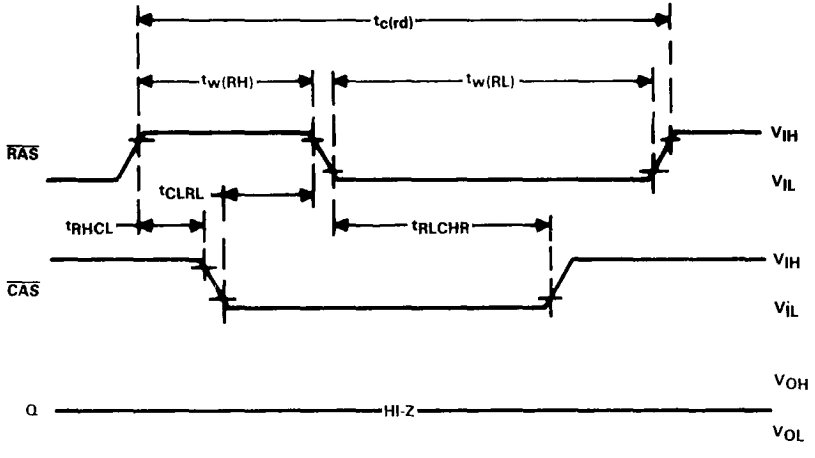
automatic ($\overline{CAS}$-before-$\overline{RAS}$) refresh cycle timing



16,384-WORD BY 4-BIT DYNAMIC RANDOM-ACCESS MEMORY

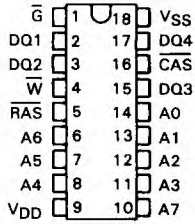
AUGUST 1980—REVISED NOVEMBER 1985

- 16,384 X 4 Organization
- Single 5-V Supply (10% Tolerance)
- Performance Ranges:

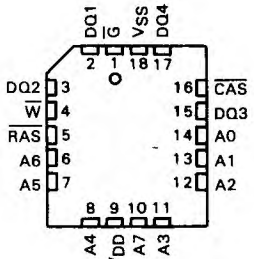
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY-WRITE CYCLE (MIN)
TMS4416-12	120 ns	70 ns	230 ns	315 ns
TMS4416-15	150 ns	80 ns	260 ns	365 ns
TMS4416-20	200 ns	120 ns	330 ns	445 ns

- Available with MIL-STD-883B Processing and L(0°C to 70°C), E(−40°C to 85°C), or S(−55°C to 100°C) Temperature Ranges
- Long Refresh Period . . . 4 ms
- Low Refresh Overhead Time . . . As Low As 1.7% of Total Refresh Period
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Unlatched Outputs
- Early Write or $\overline{G}$ to Control Output Buffer Impedance
- Page-Mode Operation for Faster Access
- Low Power Dissipation
  - Operation . . . 200 mW (Typ)
  - Standby . . . 17.5 mW (Typ)
- SMOS (Scaled-MOS) N-Channel Technology

N PACKAGE
(TOP VIEW)



FP PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ4	Data In/Data Out
$\overline{G}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TMS4416 is a high-speed, 65,536-bit, dynamic, random-access memory, organized as 16,384 words of 4 bits each. It employs state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon gate technology for very high performance combined with low cost and improved reliability.

The TMS4416 features $\overline{RAS}$ access times to 120 ns maximum. Power dissipation is 200 mW typical operating, 17.5 mW typical standby.

SMOS technology permits operation from a single 5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{DD} peaks have been reduced to 60 mA typical, and a −1-V input voltage undershoot can be tolerated, minimizing system noise considerations. Input clamp diodes are used to ease system design.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{RAS}$ can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS4416 is offered in 18-pin plastic dual-in-line and 18-lead plastic chip carrier packages. It is guaranteed for operation from 0°C to 70°C. The dual-in-line package is designed for insertion in mounting-hole rows on 7,62-mm (300-mil) centers.

operation

address (A0 through A7)

Fourteen address bits are required to decode 1 of 16,384 storage locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the six column-address bits are set up on pins A1 through A6 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable (W) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data out will remain in the high-impedance state allowing a write cycle with $\overline{G}$ grounded.

data in (DQ1 through DQ4)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In a delayed or read-modify-write cycle, $\overline{G}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

data out (DQ1 through DQ4)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ and $t_{a(G)}$ are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{G}$ are low. $\overline{CAS}$ or $\overline{G}$ going high returns it to a high-impedance state. In an early write cycle, the output is always in the high-impedance state. In a delayed-write or read-modify-write cycle, the output must be put in the high-impedance state prior to applying data to the DQ input. This is accomplished by bringing $\overline{G}$ high prior to applying data, thus satisfying t_{GHD}.

output enable ($\overline{G}$)

The $\overline{G}$ input controls the impedance of the output buffers. When $\overline{G}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{G}$ low during a normal cycle will activate the output buffers putting them

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in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state. Once in the low-impedance state, they will remain in the low-impedance state until $\overline{G}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffer is in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

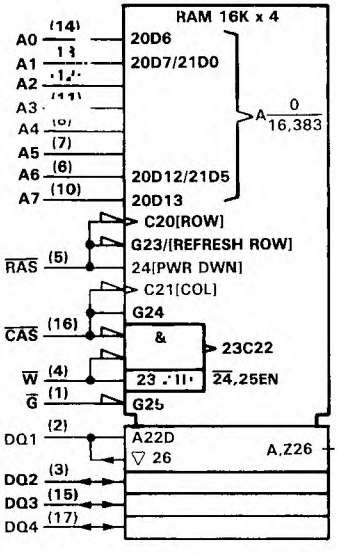
page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 64 column locations on a single RAM, the row address and $\overline{RAS}$ are applied to multiple 16K × 4 RAMs. $\overline{CAS}$ is then decoded to select the proper RAM.

power up

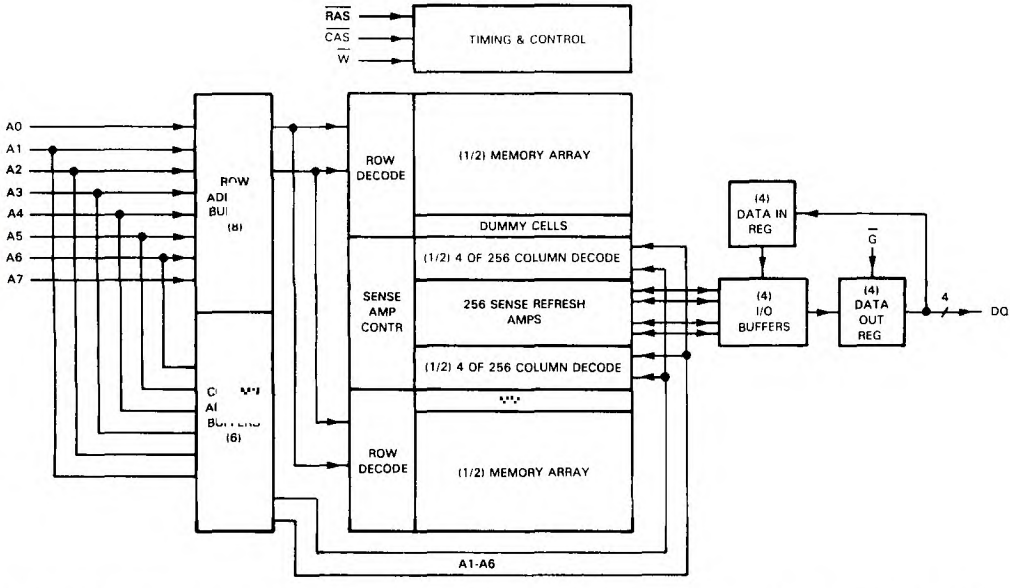
After power up, the power supply must remain at its steady-state value for 1 ms. In addition, the $\overline{RAS}$ input must remain high for 100 μs immediately prior to initialization. Initialization consists of performing eight $\overline{RAS}$ cycles before proper device operation is achieved.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std.91-1984 and IEC Publication 617-12.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range for any pin except V_{DD} and data out (see Note 1) . . . . . −1.5 V to 10 V
Voltage range for V_{DD} supply and data out with respect to V_{SS} . . . . . −1 V to 6 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values in this data sheet are with respect to V_{SS}.
2. Additional information concerning the handling of ESD sensitive devices is available in a document entitled *"Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies"* in Section 12.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		4.5	5	5.5	V
V_{SS}	Supply voltage			0		V
V_{IH}	High-level input voltage	V_{DD} = 4.5 V	2.4		4.8	V
		V_{DD} = 5.5 V	2.4		5.8	
V_{IL}	Low-level input voltage (see Notes 3 and 4)		−0.6	0	0.8	V
T_A	Operating free-air temperature		0		70	°C

NOTES: 3. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

4. Due to input protection circuitry, the applied voltage may begin to clamp at −0.6 V. Test conditions must comprehend this occurrence. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS4416-12			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −2 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5V, All other pins = 0 V			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open			54	mA
I_{DD2}	Standby current (see Note 5)	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		3.5	5	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high, All outputs open			46	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, All outputs open			46	mA

† All typical values are at T_A = 25°C and nominal supply voltages.

NOTE 5: $V_{IL} \geq -0.6V$ on all inputs. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS4416-15			TMS4416-20			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −2 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5V, All other pins = 0 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		40	48		35	42	mA
I_{DD2}	Standby current (see Note 5)	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		3.5	5		3.5	5	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high, All outputs open		25	40		21	34	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, All outputs open		25	40		21	34	mA

† All typical values are at T_A = 25°C and nominal supply voltages.
NOTE 5: $V_{IL} \geq -0.6V$ on all inputs. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs	5	7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs	8	10	pF
$C_{i(W)}$	Input capacitance, write-enable input	8	10	pF
$C_{i/o}$	Input/output capacitance, data ports	8	10	pF

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switching characteristics over recommended supply voltage range and operating free-air temperature *range*

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS4416-12 MIN	TMS4416-12 MAX	UNIT
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		70	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF, Load = 2 Series, 74 TTL gates	t_{RAC}		120	ns
$t_{a(G)}$	Access time after $\overline{G}$ low	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OEA}		30	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	30	ns
$t_{dis(G)}$	Output disable time after $\overline{G}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OEZ}	0	30	ns

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS4416-15 MIN	TMS4416-15 MAX	TMS4416-20 MIN	TMS4416-20 MAX	UNIT
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		80		120	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF, Load = 2 Series, 74 TTL gates	t_{RAC}		150		200	ns
$t_{a(G)}$	Access time after $\overline{G}$ low	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OEA}		40		50	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	30	0	40	ns
$t_{dis(G)}$	Output disable time after $\overline{G}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OEZ}	0	30	0	40	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TMS4416-12 MIN	TMS4416-12 MAX	UNIT
$t_{c(P)}$	Page-mode cycle time	t_{PC}	[illegible]		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	[illegible]		ns
$t_{c(W)}$	Write cycle time	t_{WC}	[illegible]		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	[illegible]		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time)‡	t_{CP}	40		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low§	t_{CAS}	70	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	80		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low¶	t_{RAS}	120	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	30		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	50		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	50		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	35		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	85		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	40		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	90		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	30		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	40		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	90		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	120		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	70		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write-cycle only)#	t_{CWD}	120		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	20	50	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write-cycle only)#	t_{RWD}	170		ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	−5		ns
t_{GHD}	Delay time, $\overline{G}$ high before data applied at DQ	t_{OED}	30		ns
t_{rf}	Refresh time interval	t_{REF}		4	ms

† All cycle times assume $t_t = 5$ ns.
‡ Page mode only.
§ In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time $t_{w(CL)}$.
¶ In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time $t_{w(RL)}$.
# Necessary to insure $\overline{G}$ has disabled the output buffers prior to applying data to the device.

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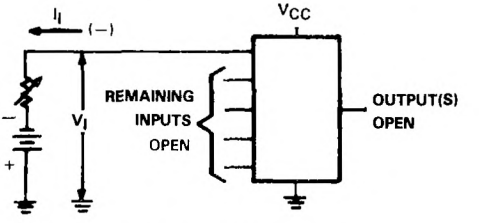
timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TMS4416-15		TMS4416-20		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time	t_{PC}	140		[illegible]		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	260		330		ns
$t_{c(W)}$	Write cycle time	t_{WC}	[illegible]		[illegible]		ns
$t_{c(rdW)}$	Read-write/read-[illegible]-write cycle time	t_{RWC}	[illegible]		[illegible]		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time)‡	t_{CP}	50		80		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low§	t_{CAS}	80	10,000	120	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	100		120		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low¶	t_{RAS}	150	10[illegible]	[illegible]	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	40		[illegible]		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	60		80		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	60		80		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	40		50		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	20		25		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	110		130		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	60		80		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	130		160		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	40		50		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		10		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(CLW)}$	[illegible]-command hold time after $\overline{CAS}$ low	t_{WCH}	60		80		ns
$t_{h(RLW)}$	[illegible]-command hold time after $\overline{RAS}$ low	t_{WCR}	130		160		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		[illegible]		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		[illegible]		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	80		120		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write-cycle only)#	t_{CWD}	120		150		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	20	70	25	80	ns
t_{RLWL}	Delay time, RAS low to $\overline{W}$ low (read-modify-write-cycle only)#	t_{RWD}	190		230		ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	−5		−5		ns
t_{GHD}	Delay time, $\overline{G}$ high before data applied at DQ	t_{OED}	30		40		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

† All cycle times assume $t_t = 5$ ns.
‡ Page mode only.
§ In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time $t_{w(CL)}$.
¶ In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time $t_{w(RL)}$.
# Necessary to insure $\overline{G}$ has disabled the output buffers prior to applying data to the device.

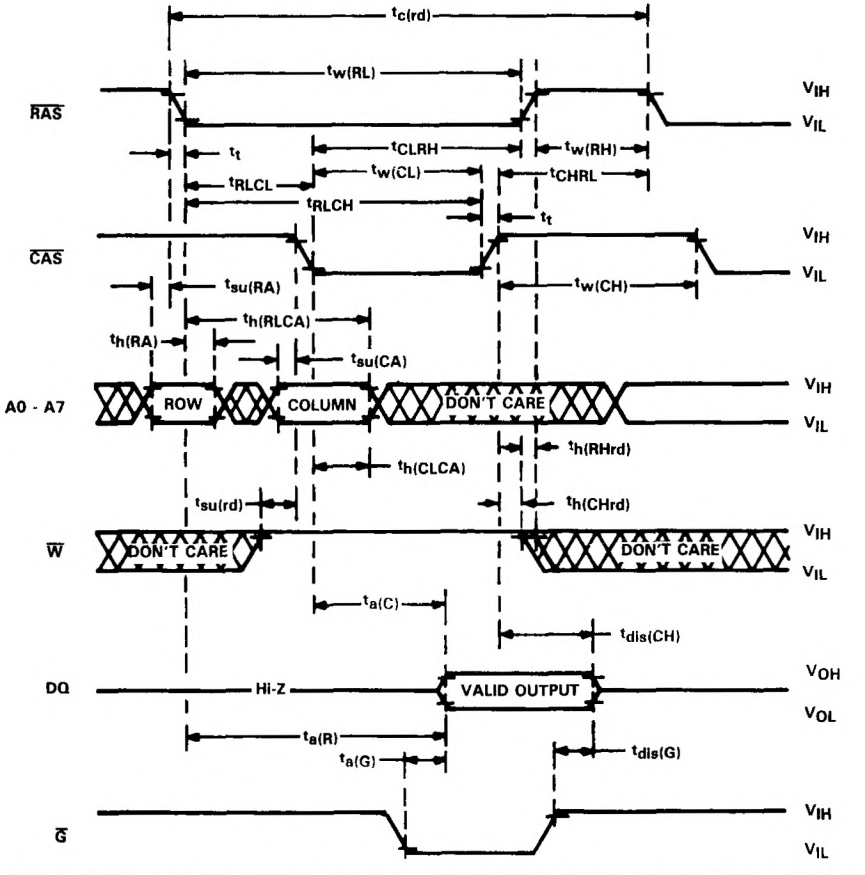
PARAMETER MEASUREMENT INFORMATION



NOTE 6: Each input is tested separately.

FIGURE 1. INPUT CLAMP VOLTAGE TEST CIRCUIT

read cycle timing



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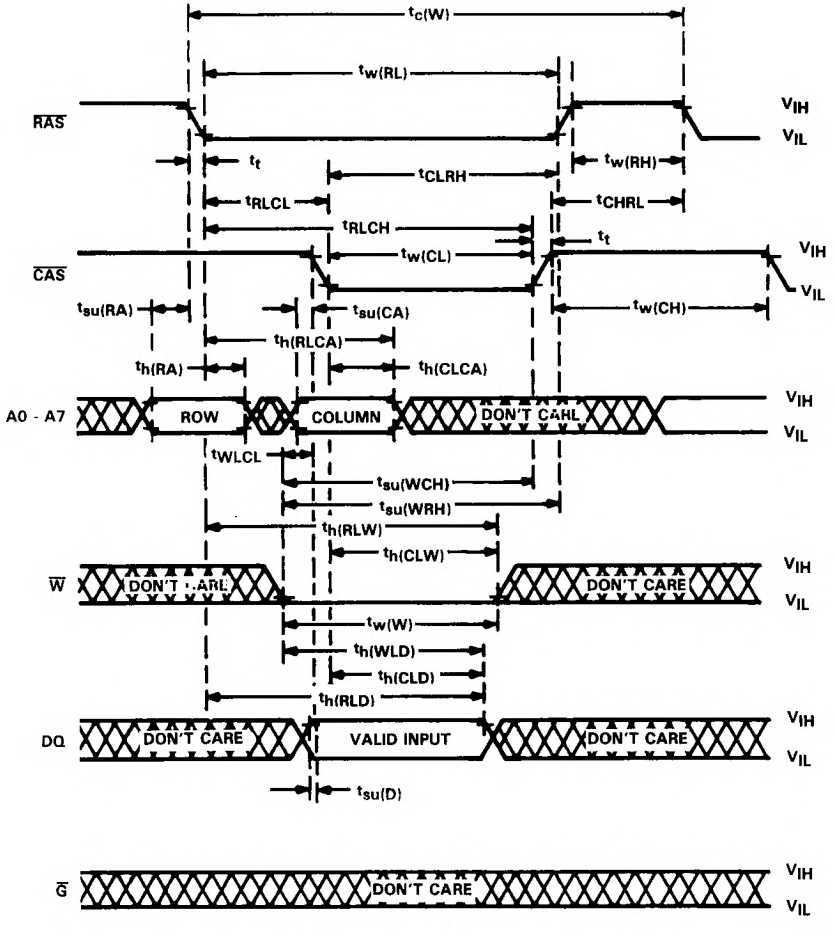
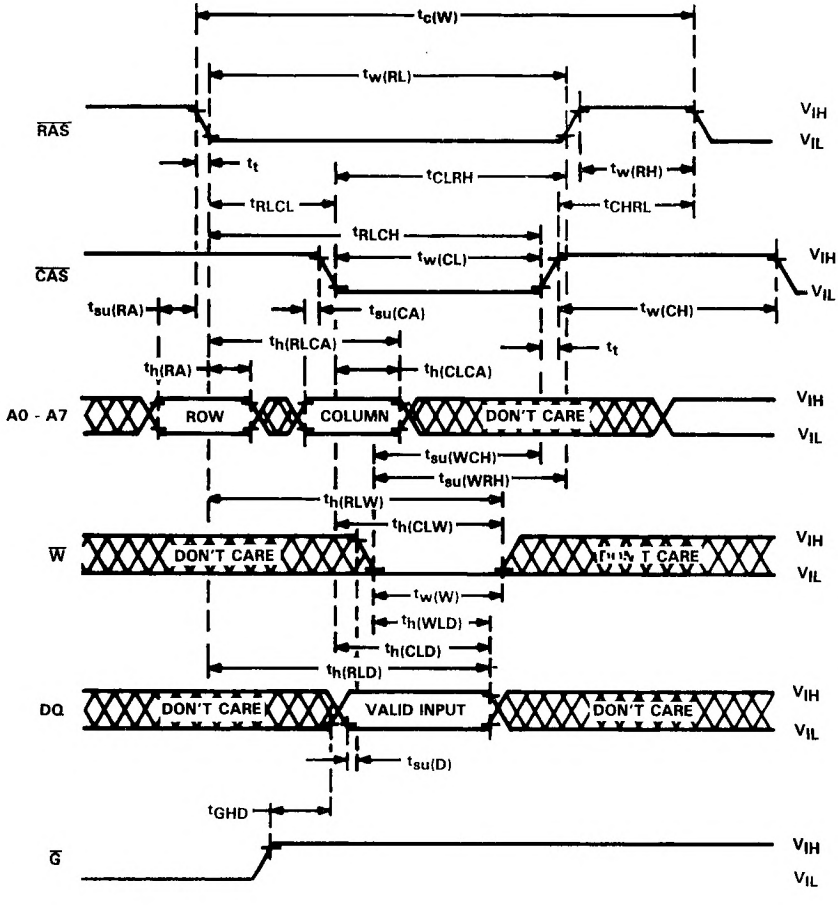
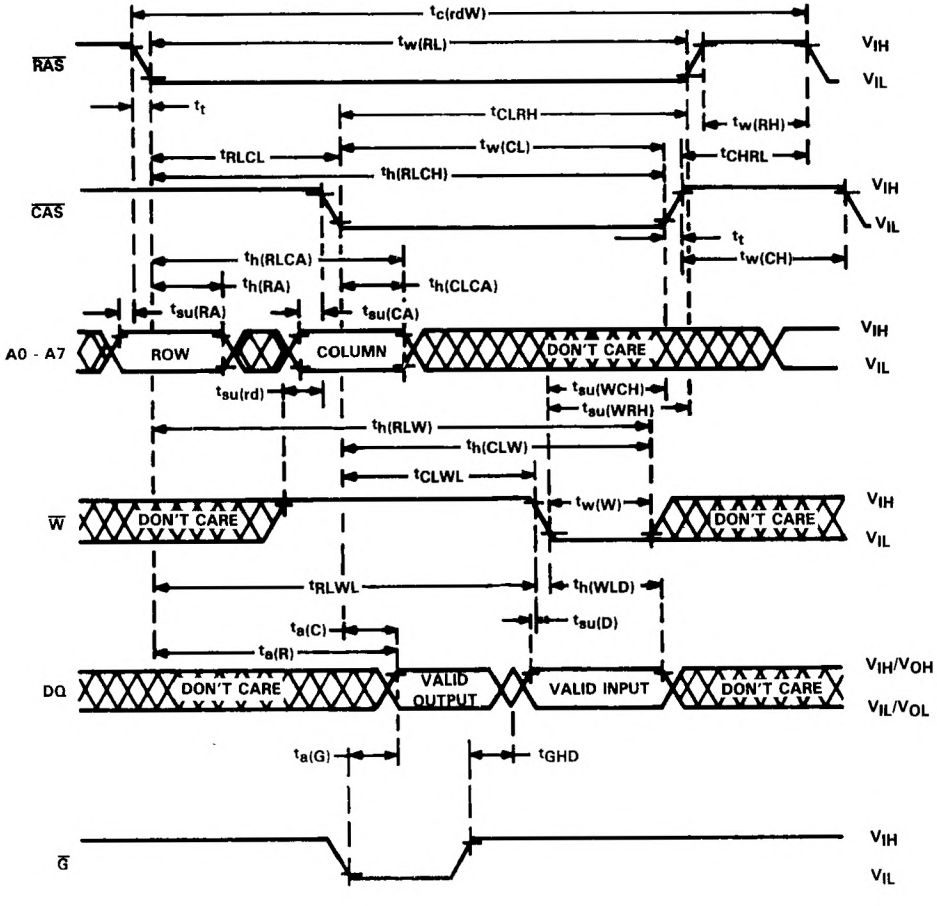
early write cycle timing



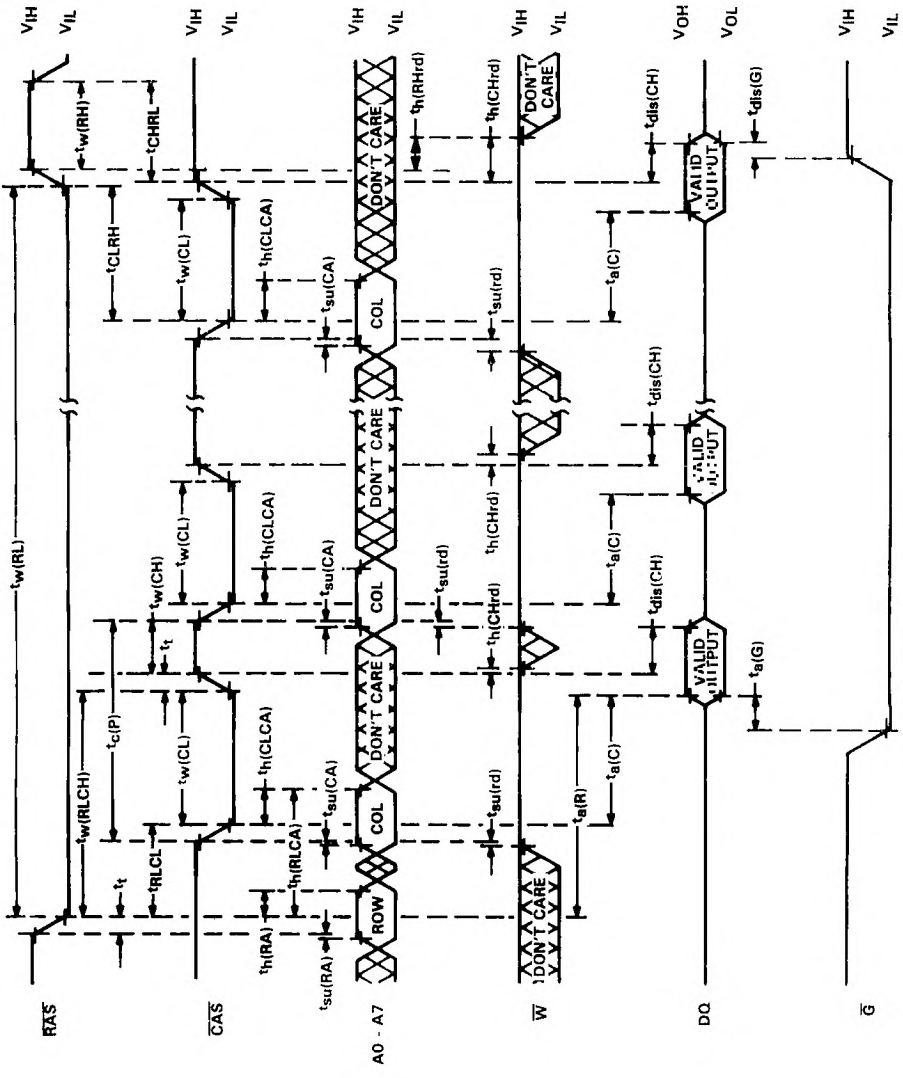
write cycle timing



read-write/read-modify-write cycle timing

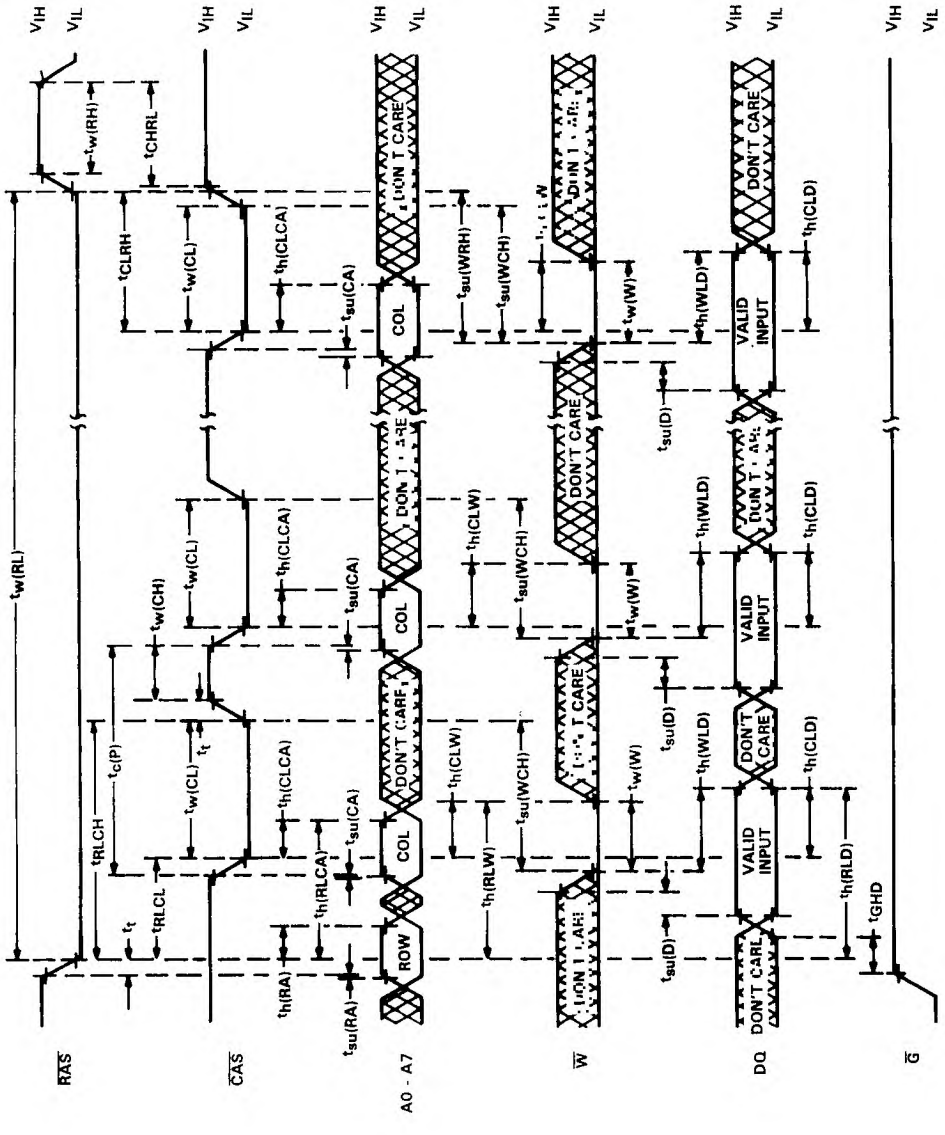


page-mode read cycle timing



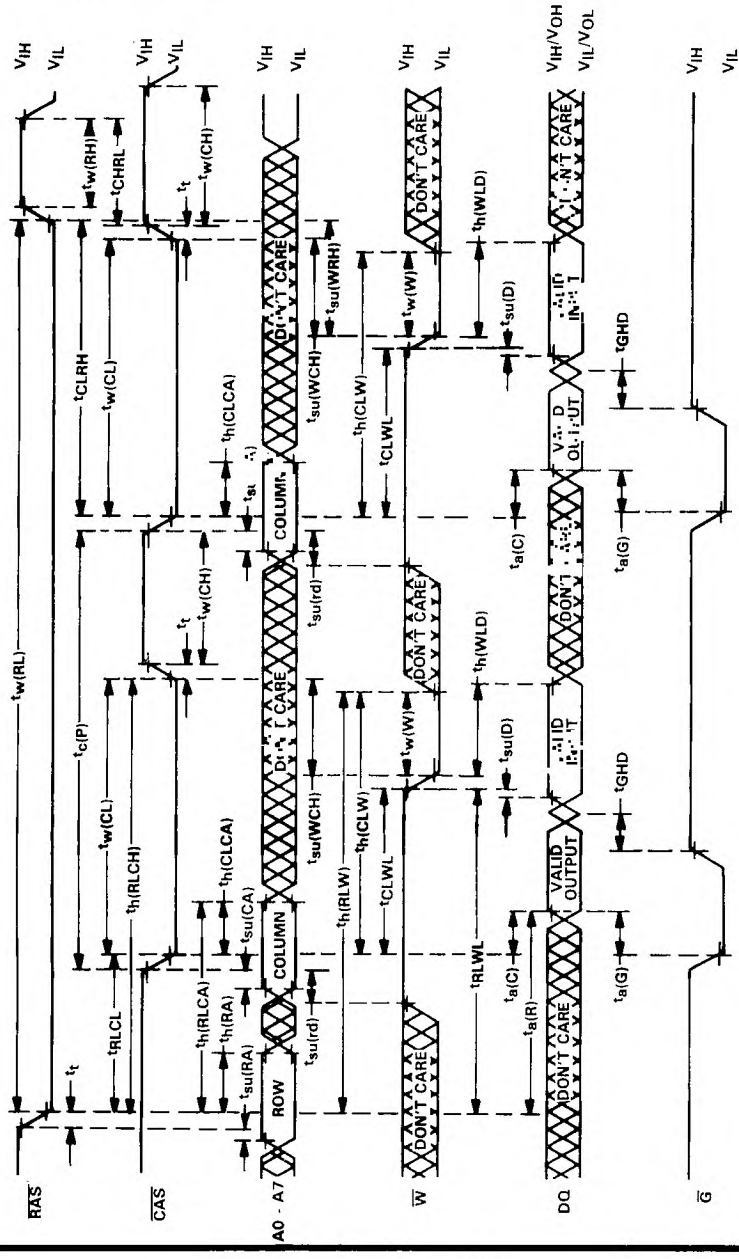
NOTE 7: A write cycle or read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

page-mode write cycle timing



NOTE 8: A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as read and read-modify-write timing specifications are not violated.

page-mode read-modify-write timing



NOTE 9: A read cycle or a write cycle can be intermixed with read-modify-write cycles as long as read and write timing specifications are not violated.

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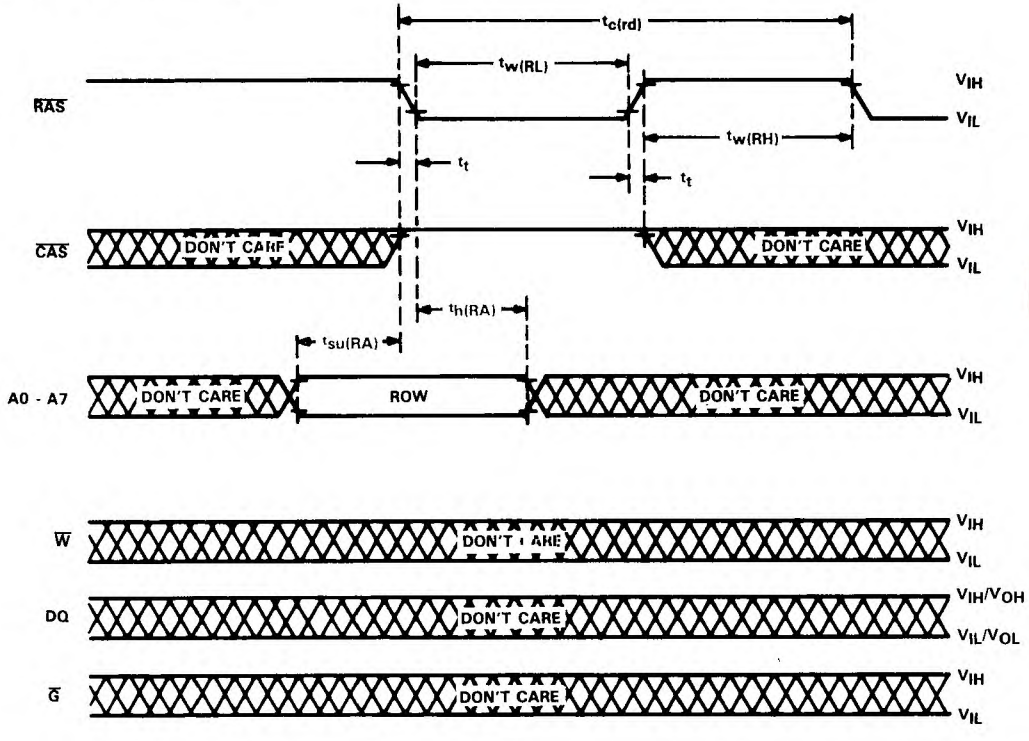
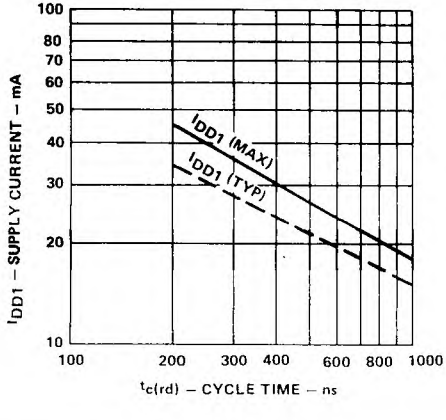
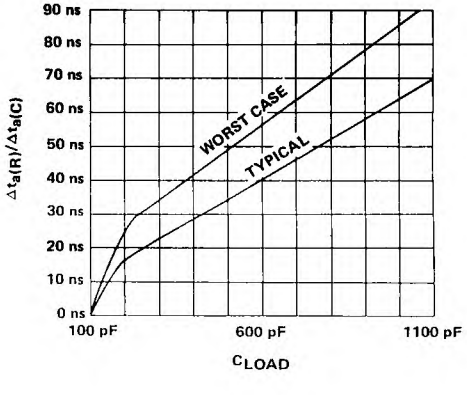
RAS-only refresh timing



I_{DD1} VS CYCLE TIME



ACCESS TIME DERATING CURVE



4

Dynamic RAMs

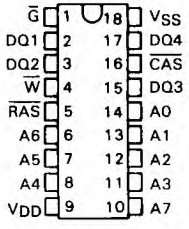
NOVEMBER 1983 – REVISED NOVEMBER 1985

- 65,536 X 4 Organization
- Single 5-V Supply (10% Tolerance)
- JEDEC Standardized Pinout
- Pinout Identical to TMS4416 (16K X 4 Dynamic RAM)
- Performance Ranges:

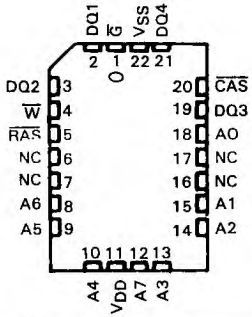
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY-WRITE CYCLE (MIN)
TMS4464-12	120 ns	60 ns	230 ns	310 ns
TMS4464-15	150 ns	75 ns	260 ns	345 ns
TMS4464-20	200 ns	100 ns	330 ns	435 ns

- Long Refresh Period . . . 4 ms (Max)
- Low Refresh Overhead Time . . . As Low As 1.3% of Total Refresh Period
- On-Chip Substrate Bias Generator
- All Inputs, Outputs, and Clocks Fully TTL Compatible
- 3-State Unlatched Output
- Early Write or $\overline{G}$ to Control Output Buffer Impedance
- Page-Mode Operation for Faster Access
- Power Dissipation As Low As:
  - Operating . . . 275 mW (Typ)
  - Standby . . . 12.5 mW (Typ)
- $\overline{RAS}$-Only Refresh Mode
- $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Mode

N PACKAGE
(TOP VIEW)



FM PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ4	Data In/Data Out
$\overline{G}$	Output Enable
NC	No Connection
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TMS4464 is a high-speed, 262,144-bit dynamic random-access memory, organized as 65,536 words of four bits each. It employs state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon/polycide gate technology for very high performance combined with low cost and improved reliability.

This device features maximum $\overline{RAS}$ access times of 120 ns, 150 ns, or 200 ns. Typical power dissipation is as low as 275 mW operating and 12.5 mW standby.

New SMOS technology permits operation from a single 5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{DD} peaks are 125 mA typical, and a −1-V input voltage undershoot can be tolerated, minimizing system noise considerations.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address and data-in lines are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS4464 is offered in 18-pin plastic dual-in-line and 22-lead plastic chip carrier packages. It is guaranteed for operation from 0°C to 70°C. The dual-in-line package is designed for insertion in mounting-hole rows on 7,62-mm (300-mil) centers.

operation

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (DQ1-DQ4)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In a delayed or read-modify-write cycle, $\overline{G}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

data out (DQ1-DQ4)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ and $t_{a(G)}$ are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{G}$ are low. $\overline{CAS}$ or $\overline{G}$ going high returns it to a high-impedance state. In a delayed-write or read-modify-write cycle, the output must be put in the high-impedance state prior to applying data to the DQ input. This is accomplished by bringing $\overline{G}$ high prior to applying data, thus satisfying t_{GHD}.

output enable ($\overline{G}$)

The $\overline{G}$ input controls the impedance of the output buffers. When $\overline{G}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{G}$ low during a normal cycle will activate the output buffers putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state. Once in the low-impedance state they will remain in the low-impedance state until $\overline{G}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every four milliseconds to retain data. This can be achieved by strobing each of the 256 rows (A0-A7). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state.

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$\overline{CAS}$-before-$\overline{RAS}$ refresh

The $\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CLRL}) and and holding it low after $\overline{RAS}$ falls (see parameter t_{RLCHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

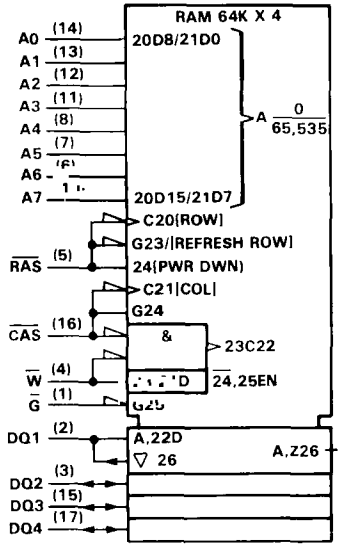
page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing random column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses for the same page is elimi[illegible] The maximum number of columns that can be addressed is determined by $t_{W(RL)}$, the maximum [illegible] low pulse duration.

power up

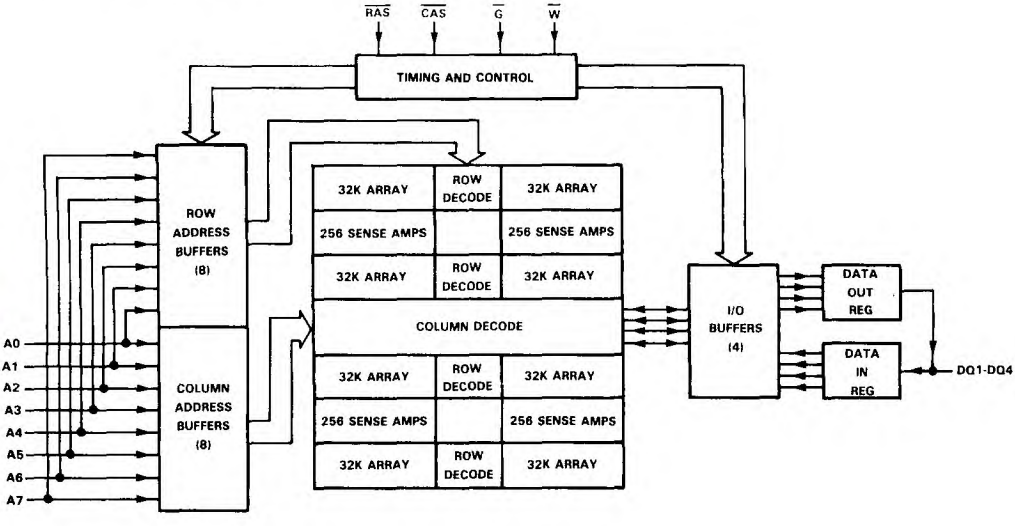
To achieve proper device operation, an initial pause of 200 μs is required after power up followed by a minimum of eight initialization cycles.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the dual-in-line package.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage on any pin including V_{DD} supply (see Note 1) . . . . . −1 V to 7 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		$V_{DD}+1$	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as maximum, is used in this data sheet for logic voltage levels only.

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electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS4464-12			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{DD} = 5 V, All other pins = 0 V to 6.5 V			±10	μA
I_O	Output current (leakage)	V_O = 0 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high, All outputs open			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle, All outputs open		65	80	mA
I_{DD2}	Standby current	After 1 memory cycle, DQ1-DQ4 held at > 0 V, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		2.5	5	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ high, All outputs open		50	60	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, All outputs open		45	55	mA

PARAMETER		TEST CONDITIONS	TMS4464-15			TMS4464-20			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{DD} = 5 V, All other pins = 0 V to 6.5 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high All outputs open			±10			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle All outputs open		55	70		50	60	mA
I_{DD2}	Standby current	After 1 memory cycle, DQ1-DQ4 held at > 0 V, $\overline{RAS}$ and $\overline{CAS}$ high, All outputs open		2.5	5		2.5	5	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ high, All outputs open		45	55		40	50	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling, All outputs open		40	50		30	40	mA

†All typical values are at T_A = 25°C and nominal supply voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		TMS4464		UNIT
		TYP†	MAX	
$C_{i(A)}$	Input capacitance, address inputs	4	7	pF
$C_{i(RC)}$	Input capacitance strobe inputs	8	10	pF
$C_{i(W)}$	Input capacitance, write enable input	8	10	pF
$C_{i/o}$	Output capacitance	8	10	pF

† All typical values are at T_A = 25 °C and nominal supply voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS4464-12		UNIT
				MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{RLCL} \geq$ MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		60	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{RAC}		120	ns
$t_{a(G)}$‡	Access time after $\overline{G}$ low	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{GAC}		35	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	30	ns
$t_{dis(G)}$	Output disable time after $\overline{G}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{GOFF}	0	30	ns

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS4464-15		TMS4464-20		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{RLCL} \geq$ MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		75		100	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{RAC}		150		200	ns
$t_{a(G)}$‡	Access time after $\overline{G}$ low	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{GAC}		45		55	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	30	0	35	ns
$t_{dis(G)}$	Output disable time after $\overline{G}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{GOFF}	0	30	0	35	ns

‡ $t_{a(C)}$ and $t_{a(R)}$ must be satisfied to guarantee $t_{a(G)}$.

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timing requirements over recommended supply voltage range and operating free-air temperature *range*

		ALT. SYMBOL	TMS4464-12 MIN	TMS4464-12 MAX	UNIT
$t_{c(P)}$	Page-mode cycle time	t_{PC}	120		ns
$t_{c(PM)}$	Page-mode cycle time (read-modify-write cycle)	t_{PCM}	200		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	230		ns
$t_{c(W)}$	Write cycle time	t_{WC}	230		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	310		ns
$t_{w(CH)P}$	Pulse duration, $\overline{CAS}$ high (page mode)	t_{CP}	50		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (non-page mode)	t_{CPN}	50		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low‡	t_{CAS}	60	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	100		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low§	t_{RAS}	120	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	40		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		ns
$t_{su(WCL)}$	Early-write command setup time before $\overline{CAS}$ low	t_{WCS}	0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	40		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	40		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	20		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	80		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	35		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	95		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	35		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	35		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	95		ns

Continued next page.

†All cycle times assume t_t = 5 ns.

‡In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$).

§In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

timing requirements over recommended supply voltage range and operating free-air temperature range (continued)

		ALT. SYMBOL	TMS4464-12 MIN	TMS4464-12 MAX	UNIT
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high¶	t_{CHR}	25		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	120		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low¶	t_{RCP}	0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	60		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)#	t_{CWD}	95		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low¶	t_{CSR}	25		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	60	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)#	t_{RWD}	155		ns
t_{GHD}	Delay time, $\overline{G}$ high before data applied at DQ	t_{GDD}	30		ns
t_{rf}	Refresh time interval	t_{REF}		4	ms

¶ $\overline{CAS}$-before-RAS refresh option only.
# $\overline{G}$ must disable the output buffers prior to applying data to the device.

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timing requirements over recommended supply voltage range and operating free-air temperature range (continued)

		ALT. SYMBOL	TMS4464-15 MIN	TMS4464-15 MAX	TMS4464-20 MIN	TMS4464-20 MAX	UNIT
$t_{c(P)}$	Page-mode cycle time	t_{PC}	145		190		ns
$t_{c(PM)}$	Page-mode cycle time (read-modify-write cycle)	t_{PCM}	230		295		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	260		330		ns
$t_{c(W)}$	Write cycle time	t_{WC}	[illegible]		[illegible]		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	345		435		ns
$t_{w(CH)P}$	Pulse duration, $\overline{CAS}$ high (page mode)	t_{CP}	60		80		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (non-page mode)	t_{CPN}	60		80		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low‡	t_{CAS}	75	10,000	100	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	[illegible]		[illegible]		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low§	t_{RAS}	[illegible]	10,000	[illegible]	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	45		55		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCL)}$	Early-write command setup time before $\overline{CAS}$ low	t_{WCS}	0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	45		60		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	45		60		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	25		45		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	15		20		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	100		145		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	45		55		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	120		155		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	45		55		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high	t_{RRH}	10		15		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	45		55		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	120		155		ns

Continued next page.

†All cycle times assume t_t = 5 ns.

‡In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$).

§In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

timing requirements over recommended supply voltage range and operating free-air temperature range (concluded)

		ALT. SYMBOL	TMS4464-15		TMS4464-20		UNIT
			MIN	MAX	MIN	MAX	
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high¶	t_{CHR}	30		35		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{RHCL}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low¶	t_{RCP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	75		100		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle)#	t_{CWD}	110		140		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low¶	t_{CSR}	30		35		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	75	30	100	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)#	t_{RWD}	185		240		ns
t_{GHD}	Delay time, $\overline{G}$ high before data applied at DQ	t_{GDD}	30		35		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

¶$\overline{CAS}$-before-$\overline{RAS}$ refresh option only.
#$\overline{G}$ must disable the output buffers prior to applying data to the device.

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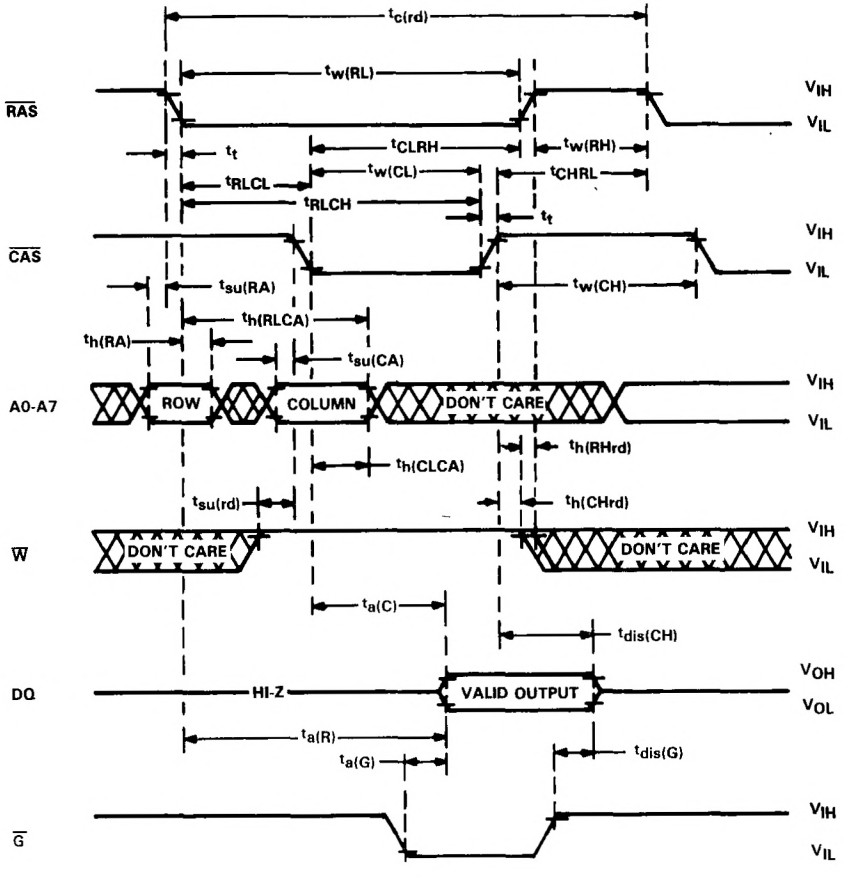
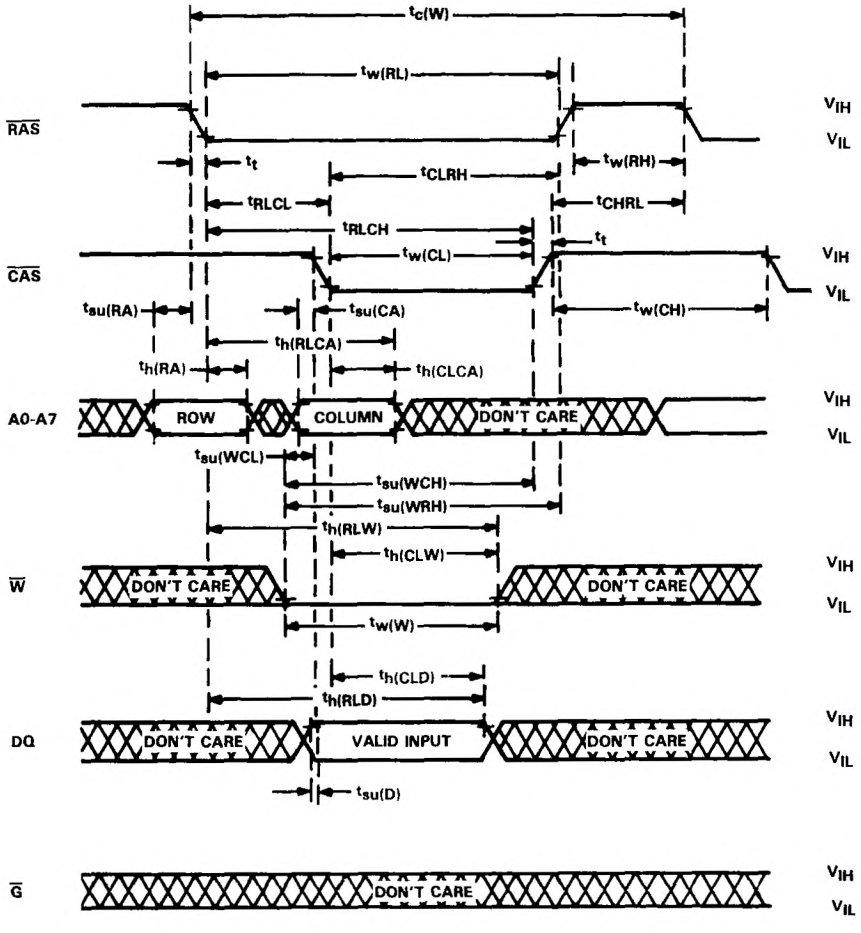
read cycle timing



early write cycle timing



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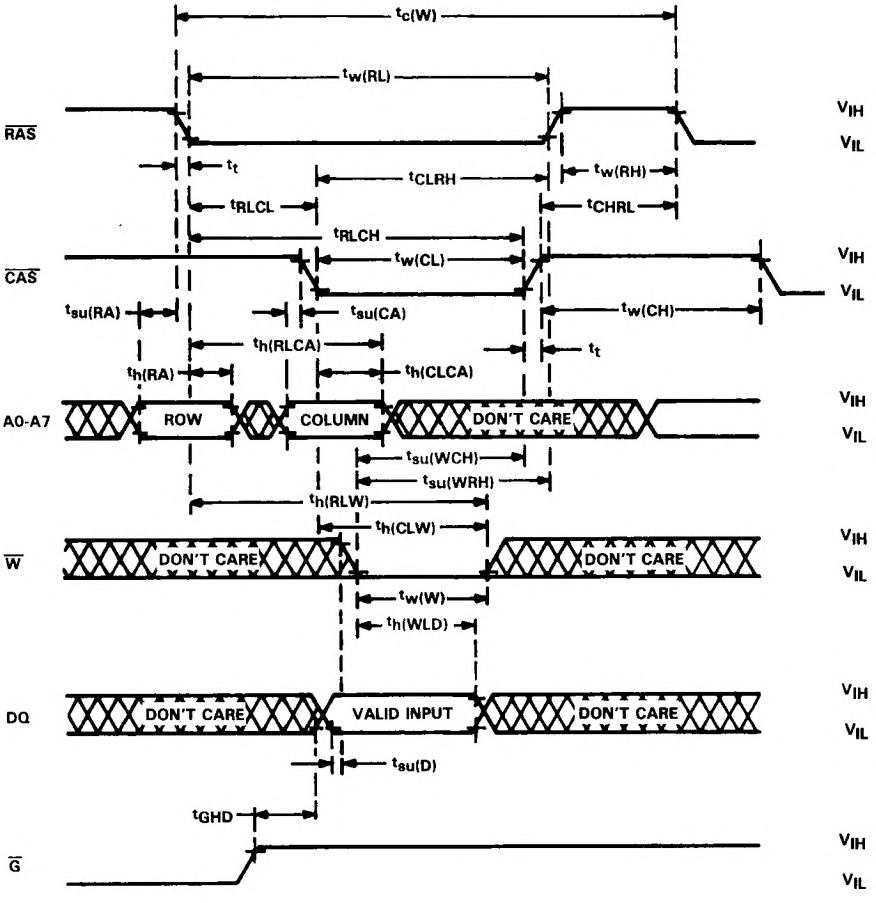
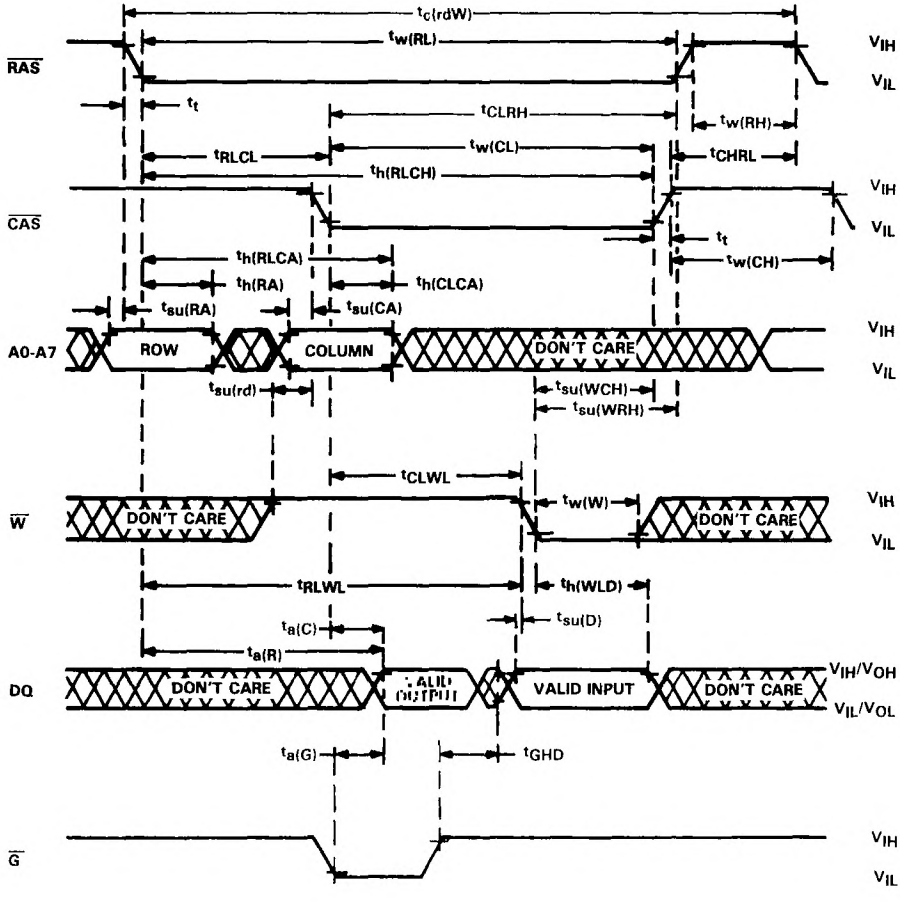
write cycle timing



read-write/read-modify-write cycle timing



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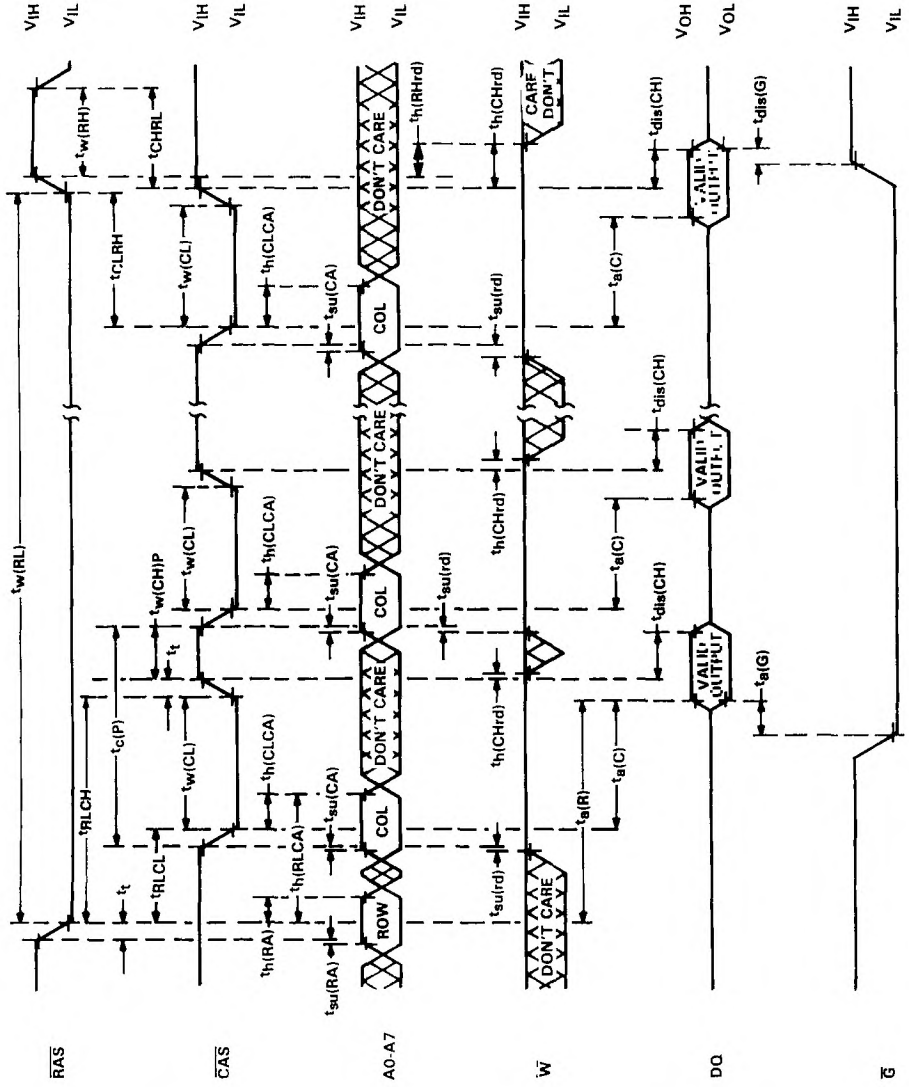
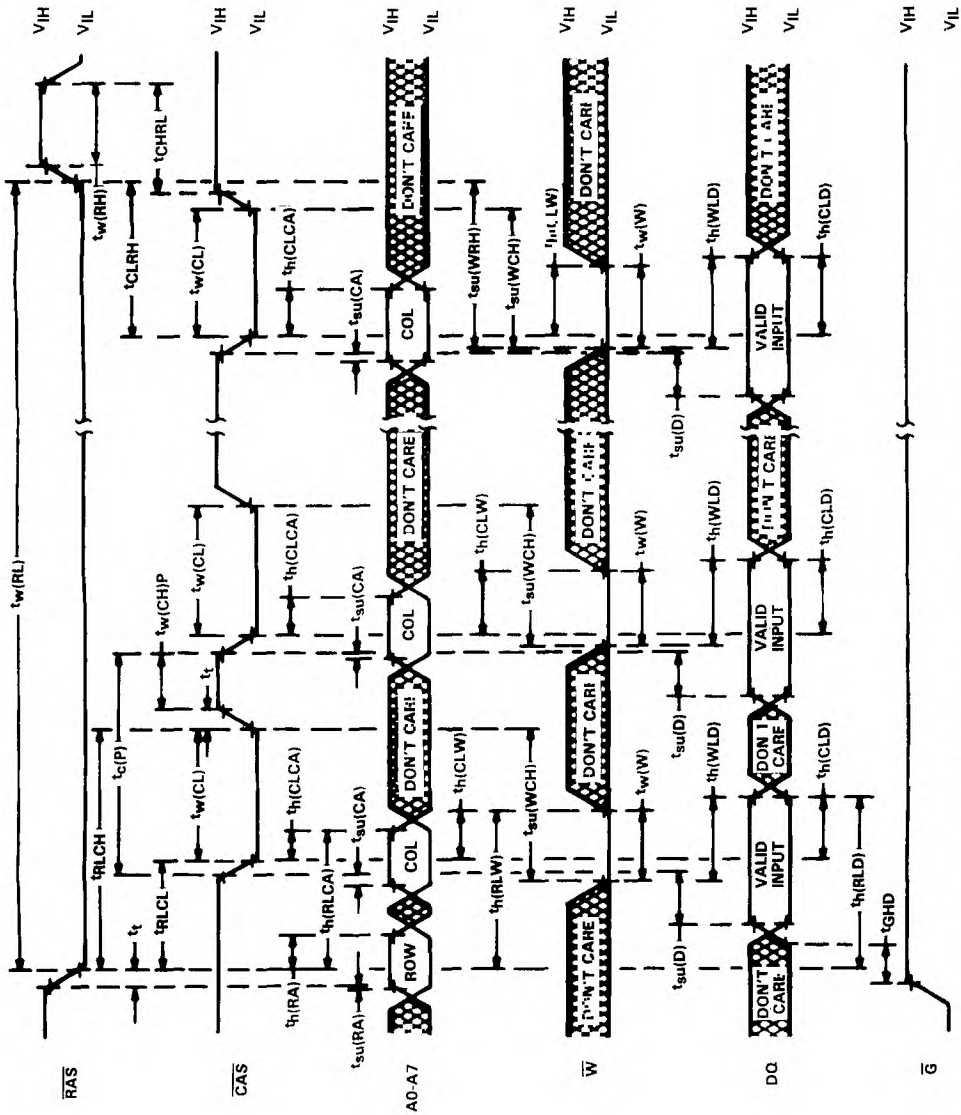
page-mode read cycle timing



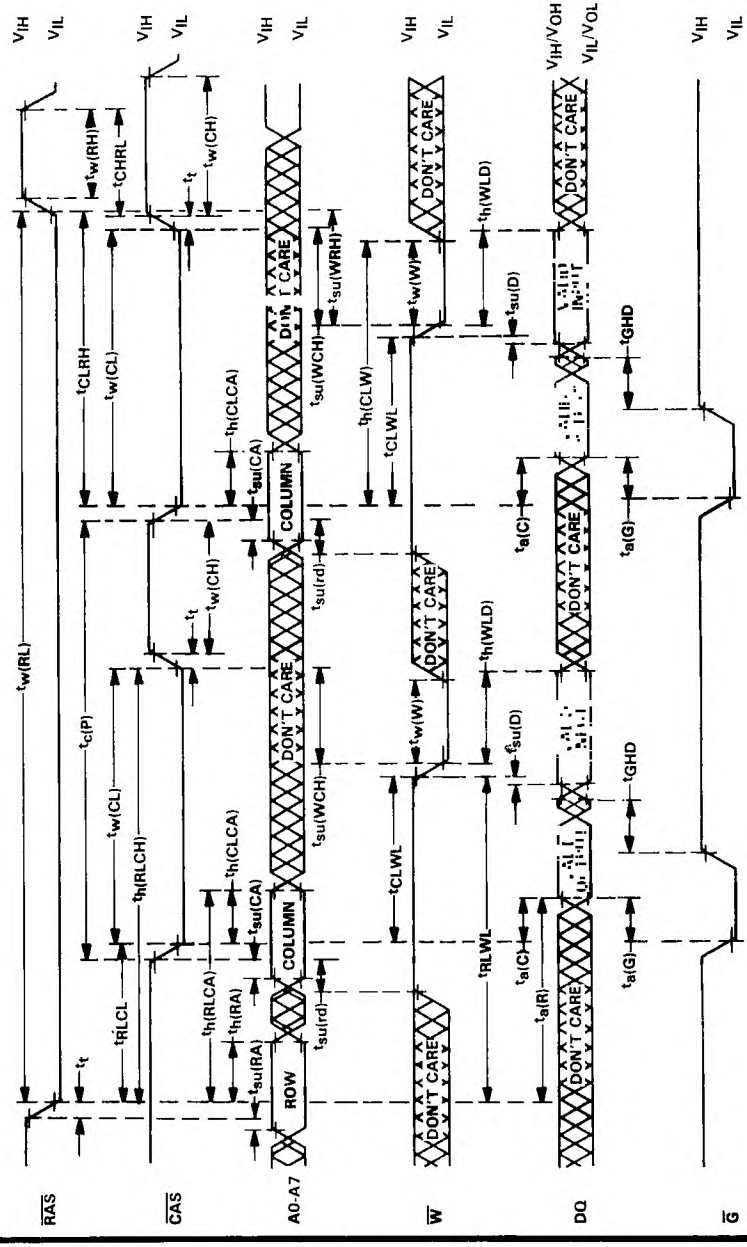
NOTE 3: A write cycle or read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

page-mode write cycle timing



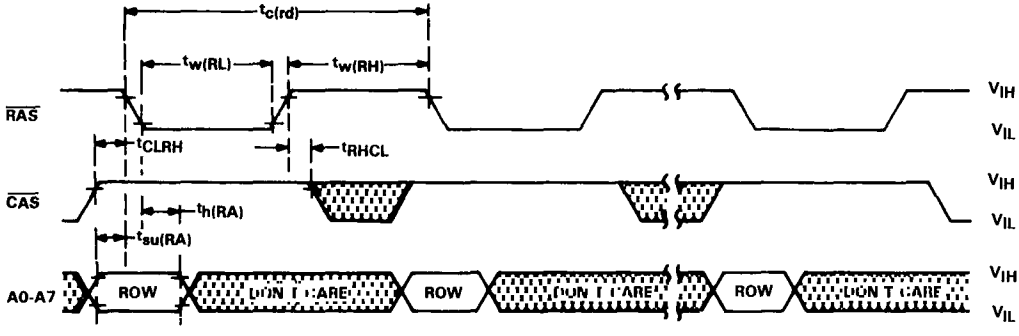
NOTE 4: A read cycle or a read-modify write cycle can be intermixed with write cycles as long as read and read-modify-write timing specifications are not violated.

page-mode read-modify-write cycle timing

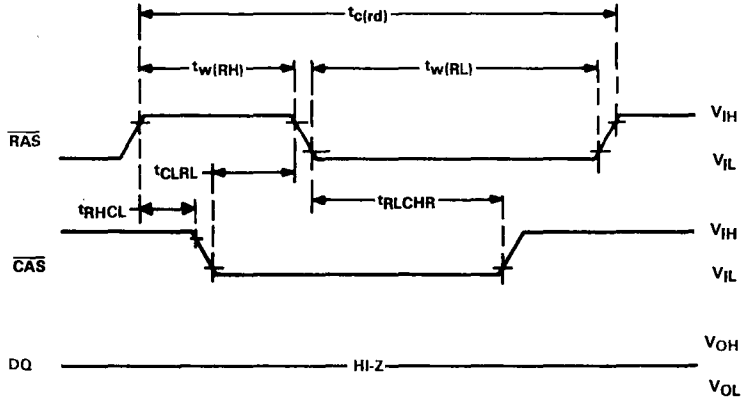


NOTE 5: A read cycle or a write cycle can be intermixed with read-modify-write cycles as long as read and write timing specifications are not violated.

$\overline{RAS}$-only refresh cycle timing



$\overline{CAS}$-before-$\overline{RAS}$ refresh cycle timing



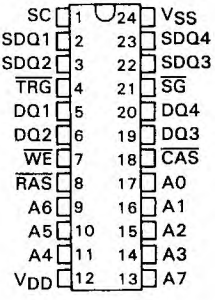
TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

TMX4461
262,144-BIT MULTIPORT VIDEO RAM

NOVEMBER 1985

- 65,536 X 4 Organization
- Dual-Port Accessibility — Four I/O's for Sequential Access, Four I/O's for Random Access
- One Serial Data Register Built into Each Serial I/O for Sequential-Access Applications
- Fast Serial Ports . . . 30-MHz Shift Rate
- Mid-Scan Load — Serial Data Streams Uninterrupted by Register Reload
- $\overline{TRG}$ as Output Enable Allows Direct Connection of DQ and Address Lines to Simplify System Design
- Random-Access Port Is Compatible with the TMS4464, 64K X 4 DRAM
- 3-State Serial I/O's Allow Easy Multiplexing of Video Data Streams
- Maximum Access Time from $\overline{RAS}$ . . . 120 ns
- Minimum Cycle Time (Read or Write) . . . 200 ns
- Long Refresh Period . . . 4 ms
- Low Refresh Overhead Time . . . As Low As 1.3% of Total Refresh Period
- All Inputs, Outputs, Clocks Fully TTL Compatible
- Three-State Unlatched Random-Access Outputs
- Common Random-Access I/O Capability with "Early Write" Feature
- High-Speed Page-Mode Operation for Faster Access
- $\overline{CAS}$-Before-$\overline{RAS}$ Refresh and Hidden Refresh Modes

N PACKAGE
(TOP VIEW)



PIN NOMENCLATURE

A0-A7	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ4	Random-Access Data In/ Data Out/Write-Mask Bit
$\overline{RAS}$	Row-Address Strobe
SC	Serial Data Clock
SDQ1-SDQ4	Serial Data In/Data Out
$\overline{SG}$	Serial Output Enable
$\overline{TRG}$	Transfer Register/ Q Output Enable
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{WE}$	Write-Mask Select/ Write Enable

- Low Power Dissipation —Operating . . . 250 mW (Typical, DRAM Port)
- 24-Pin, 400-Mil Dual-in-Line Package

description

The 256K Multiport Video RAM is a high-speed dual-ported 65,536 × 4 bit dynamic random-access memory with on-chip data registers. The random-access port makes the memory look like it is organized as 65,536 words of four bits each like the TMS4464. The sequential-access port is interfaced to four internal 256-bit dynamic data registers which make the memory look like it is organized as 256 four-bit words of up to 256 bits each which are accessed serially.

The 256K Multiport Video RAM employs state-of-the art double-level polysilicon/polycide gate technology for very high performance combined with low cost and improved reliability.

TMX44C256, TMX44C257, TMX44C259
262,144-WORD BY 4-BIT DYNAMIC RANDOM-ACCESS MEMORIES

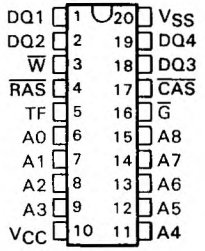
NOVEMBER 1985

- 262,144 X 4 Organization
- Single 5-V Supply (10% Tolerance)
- Pinout to Proposed JEDEC Standard
- Performance Ranges:

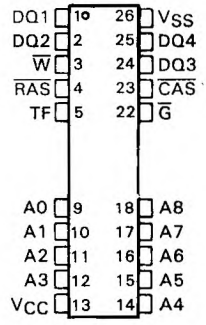
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)
TMX44C25_-10	100 ns	50 ns	200 ns
TMX44C25_-12	120 ns	60 ns	230 ns
TMX44C25_-15	150 ns	75 ns	260 ns

- Multiple Operations Options:
  TMX44C256 — Page Mode/Enhanced Page Mode
  TMX44C257 — Static Column Mode
  TMX44C259 — 256 X 4 Bit Nibble Mode (Serial Mode)
- Long Refresh Period
  512-Cycle Refresh in 8 ms (Max)
- Three-State Unlatched Output
- Lower Power Dissipation
- New Scaled-CMOS Technology
- Low Standby Power with CMOS-Level Inputs
- High-Reliability Plastic 20-Pin 300-Mil-Wide DIP or Surface-Mount Packages

N PACKAGE
(TOP VIEW)



DJ PACKAGE†
(TOP VIEW)



†The packages shown here are for pinout reference only. The DJ package is actually 75% of the length of the N package.

description

The Megabit DRAM devices are high-speed, 1,048,576-bit dynamic random-access memories organized as 262,144 words of four bits each. They employ state-of-the-art TIC-MOS (Scaled CMOS) technology for high performance, reliability and lower power at a low cost.

PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ4.	Data In/Data Out
$\overline{G}$	Data Output Enable
$\overline{RAS}$	Row-Address Strobe
TF	Test Function
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

TMX4C1024, TMX4C1025, TMX4C1026, TMX4C1027, TMX4C1029
1,048,576-BIT DYNAMIC RANDOM-ACCESS MEMORIES

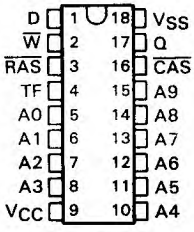
NOVEMBER 1985

- 1,048,576 X 1 Organization
- Single 5-V Supply (10% Tolerance)
- Pinout to Proposed JEDEC Standard
- Performance Ranges:

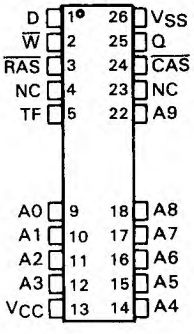
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)
TMX4C102_-10	100 ns	50 ns	200 ns
TMX4C102_-12	120 ns	60 ns	230 ns
TMX4C102_-15	150 ns	75 ns	260 ns

- Multiple Operations Options:
  - TMX4C1024 — Page Mode/Enhanced Page Mode
  - TMX4C1025 — 4-Bit Nibble Mode
  - TMX4C1026 — 8-Bit Nibble (Byte)
  - TMX4C1027 — Static Column Mode
  - TMX4C1029 — 1024-Bit Nibble Mode (Serial Mode)
- Long Refresh Period
  512-Cycle Refresh in 8 ms (Max)
- Three-State Unlatched Output
- Lower Power Dissipation
- New Scaled-CMOS Technology
- All Inputs and Clocks Are TTL Compatible
- Low Standby Power with CMOS-Level Inputs
- High-Reliability Plastic 18-Pin 300-Mil-Wide DIP or Surface-Mount Packages

N PACKAGE
(TOP VIEW)



DJ PACKAGE†
(TOP VIEW)



†The packages shown here are for pinout reference only. The DJ package is actually 75% of the length of the N package.

PIN NOMENCLATURE	
A0-A9	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data In
NC	No Connection
Q	Data Out
$\overline{RAS}$	Row-Address Strobe
TF	Test Function
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

description

The Megabit DRAM devices are high-speed, 1,048,576-bit dynamic random-access memories organized as 1,048,576 words of one bit each. They employ state-of-the-art TIC-MOS (Scaled CMOS) technology for high performance, reliability and lower power at a low cost.